Alumina Ceramics Preperation and its Properties for Electronics Uses

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Abstract

Electronics curcuit systems tend to densify, to be small and even higher performance. Electrical wiring density of these systems increases, depending on the requirement. It has been recognized which alumina ceramic multi-layer boards are matched to it, because of the fine line wiring.

Electrical signal transmission through the wiring on these boards takes a certain time that is signal delay. High speed signal processor needs to make the high speed transmission wiring. The delay is affected by the dielectric around the wiring as the relation of $Tdp = 1 \cdot \varepsilon r / c$. Where, Tdp is the delay, 1 is the wiring lengh εr is the specific dielectric constant and c is light speed. Therefore, the reducing dielectric constant of alumina ceramics is promoting to study now.

Table 1 show the recent new material for the cofired multilayer board in high performance computers. Almost of these are in alumina based. The doctor-blade tape casting method still continue to use for them. Glass contained alumina bodies decrease their firing temperature, and weaken their strength. These make the difficulty of the buru-out of binders, and control void distribution. Each problem is improving to produce cofired multilayer boards with precised fine dimension.

1. Interconnection of circuits

Electronics circuit systems are owing much of the growing semiconductor

devices which are IC and LSI's. Interconnection between the LSI's, that is called as LSI packaging, is also progressed by the requirements. Certain wiring boards which are the most significant parts have been utilized as these packages.

The electrical signal transmission through the wiring in this board takes a certain time that is the signal delay. This delay is affected by the dielectrics among the wiring as following relations:

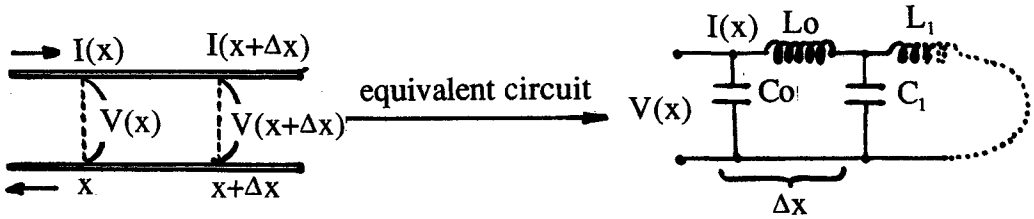


Figure 1 Model of transmission lines

Figure 1 shows a typical signal propagation lines in the specified dielectrics. Electrical current and potential differences (voltage) are the representative of energy. Where, the voltage at x point is V(x) and the current at x point is I(x). If the current is changing, the inductance (Lo) at the differencial distance (Δ x) induce the voltage drop (ΔV) that is given as

$$\Delta V = V(x+\Delta x) - V(x) = -Lo\Delta x\frac{dI}{dt} \quad \text{---------- (1)}$$

when the Δx is to limit as zero

$$\frac{\partial V}{\partial x} = -Lo\frac{\partial I}{\partial t} \quad \text{---------- (2)}$$

is derived. The changing current gives the slope of voltage.

When the voltage is changing at x, the capacitance Co at the differencial distance (Δx) charges the electrical load q=CoΔxV. This load changing rate is CoΔxdV/dt. Which makes the difference in the current (ΔI) between input at x and out put at x+Δx. That is given as

$$\Delta I = -Co\Delta x\frac{dV}{dt} \quad \text{---------- (3)}$$

At limit of $\Delta x \rightarrow o$,

$$\frac{\partial I}{\partial x} = -Co\frac{\partial V}{\partial t} \quad \text{---------- (4)}$$

electric is charged.

For delete the ∂I or ∂V on the above two partial differntial equations, the right term makes differential again by x and the left term does the same by t respectively.

$$\frac{\partial^2 V}{\partial x^2} = CoLo \frac{\partial^2 V}{\partial x^2}$$

$$\frac{\partial^2 I}{\partial x^2} = CoLo \frac{\partial^2 I}{\partial t^2} \quad \text{---------- (5)}$$

are formed. $\alpha^2 x / \alpha t^2$ is the squared velocity (u^2). Then the above equation can be deformed as

$$\frac{\partial x}{\partial t} = u^2 = \frac{1}{LoCo}, \; u = \frac{1}{\sqrt{LoCo}} \quad \text{---------- (6)}$$

The Lo and Co are the function of the dielectric material. Therefore, the propagation velocity of the puls energy is represented by the specific dielectric constant (ε r) and magnetic constant (μ r).

$$u = \frac{1}{\sqrt{LoCo}} = \frac{1}{\sqrt{\varepsilon r.\mu r}} \cdot \frac{1}{\sqrt{\varepsilon o.\mu o}} = \frac{c}{\sqrt{\varepsilon r.\mu r}} \quad \text{---------- (7)}$$

where c is light velocity, ε o is dielectric constant in vaccum, and μ o is magnetic as well. In usual case μ r $\simeq$1, this equation is simplified as

$$u = \frac{c}{\sqrt{\varepsilon r}} \quad \text{---------- (8)}$$

We recognize as the signal propagation delay depends on the surrounded material and transmission distance .

$$Tpd = \frac{x}{u} = \frac{\sqrt{\varepsilon r} \cdot x}{c} \quad \text{---------- (9)}$$

Figure 2 shows the distance between the cell units that is wiring length, related with the signal propagation delay. The switching speed of the transistor units in silicon LSI is limited by their carrier migration speed in silicon material. Therefore, Si LSI chips position at upper right hand side of the carrier speed in Fngure 2. Wiring in the LSI package has higher speed that is $c/\sqrt{\varepsilon}r$. This shares the position at nearer line of light speed limit, but enlarges the delay due to increase the wiring length. System cards or boads are more adjacent to it as the similar concept. And also a transistor to another transistor distance (x) apparently expands to far distance. Therefore, the delay increases with the propotion of the $\sqrt{\varepsilon}rx$ / c.

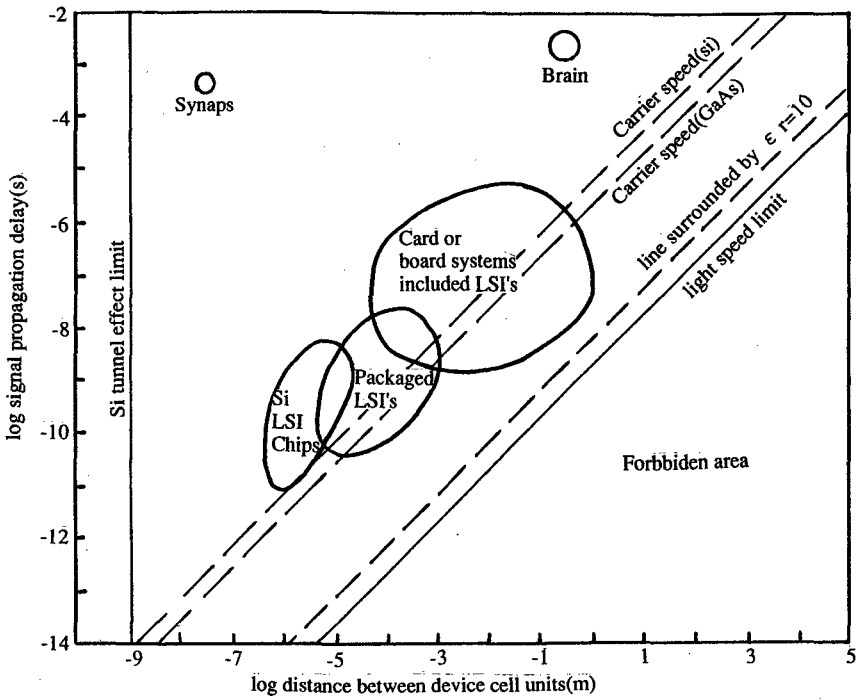


Figure 2 Relation between distance of each unit cell and signal delay

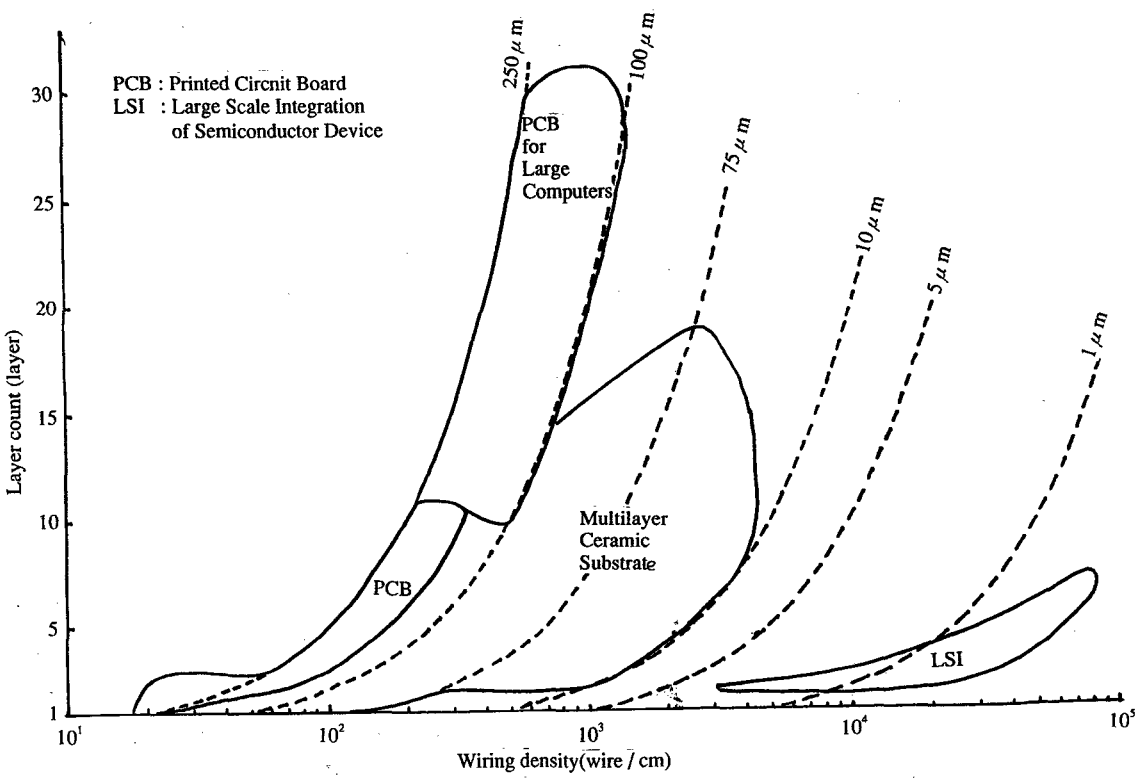


Figure 3 Comparison of wiring densities on their production processed

To produce the shorter wiring that means getting smaller delay, finner pattern processing is required. This is a essential concept for electronics system.
Figure 3 shows the comparison of the wiring density depending on their production processes. Finest wiring density is found in LSI processing, which of value shares for 10^4 to 10^5 on several layers. In other part, the technology of plastic printed circuit boards (PCB) produce only the 10^1 to 10^2 wiring, and even the heavily stacked layer ones have only less than 10^3 wiring. There is a great difference between the two processes. The ceramic multlayer board process is relatively better than PCB for the wiring density as shown in Figure 3. This is a reason why ceramic multilayer boards are used for high density circuits such as large computers. Requirement of this technology is to reduce the dielectric constant of the ceramics and wiring dimensions.

2. Low dielectric constant

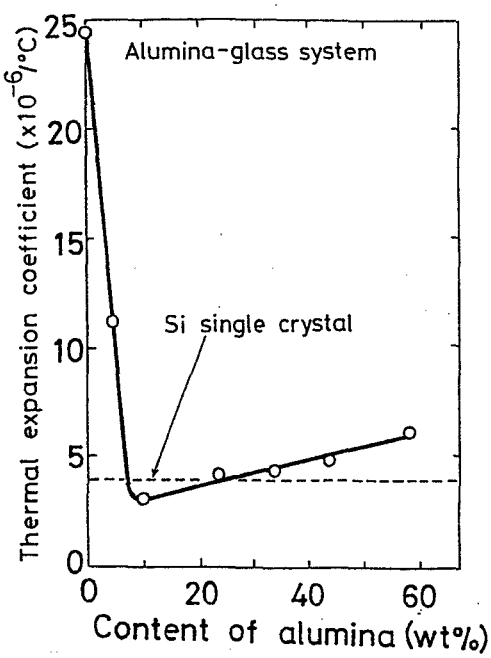
Table 1[1)] shows the recent new materials for the cofired multilayer boards in high performance computers. General recognition is that ceramics is higher in dielectric constants than plastic ones. Lowest dielectric constant indicates in silica glass as far as conventional material choice. Therefore, new materials generally include much silica quantity.

Alumina still remaines as the major composition to keep the high mechanical strength of the ceramic bodies. Alumina-glass system makes one group. Other find in mullite glass system. The 3.5 to 5.9 of dielectric constants are introduced by these new material systems, which compare with the 9.0 to 10.0 of alumina values. Change of alumina or mullite content in silica glass and borosilicate glass affects to the characteristics of the final products. Large volume of the ceramic filler tends to improve the mechanical strength and thermal conductivity. Otherwise, large volume of the glass reduces the dielectric constant and thermal mismatch with silicon chips due to decrease the difference between them of the thermal expansion coefficent(TEC). This trade-off is controlled for the products. Therefore, the arround 5 of dielectric constant is given as the results. For examples, Imanaka et al[2)] was pointed out that the alumina-borosilicate glass system induced the cristobalite in the low content of alumina, which indicated high TEC as shown in Figure 4. And the mullite-borosilicate system also made it

as similar as the alumina system[3] as shown in Figure 4. Therefore the higher content of filler material was adopted to the products, which gave good mechanical strength as shown in Figure 54). mechanical strength as shown Figure 5 [4]

Table 1. Recent Ceramic Multilayer Board

Material	Rough Compositon	Dielectric Constant	Thermal Expansion Coefficient (ppm)	Modulus of Rapture (Mpa)	Wiring Metal	Maker
Alumina-Glass System	Al2O3 18-23, SiO2 55-55, MgO 18-25, P2O5, B2O3	5.2	3.0	210	Cu	IBM
	Alumina, Borosilicate Glass	5.6	4.0	200	Cu	Fujitsu
	Photosensitive Alumina-Glass	3.5			Au	NEC
Mullite	Mullite, Glass	5.9	3.5	200 or more	W	Hitachi
Alumina	~95% Alumina	9.0 ~10.0	6.0	300 or more	W	Reference



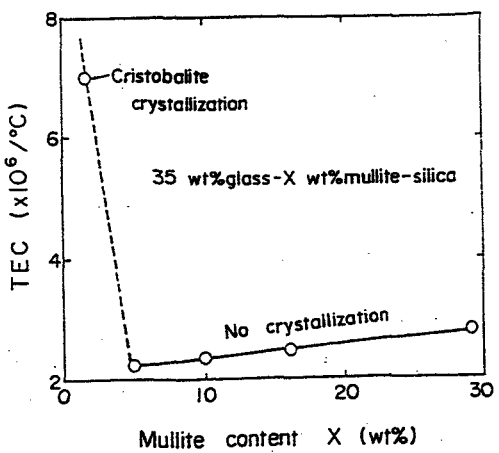


Figure 4. Relation between TEC of glass/ceramic composites and amounts of alumina addition[2] and Mullite addition[3] (right graph)

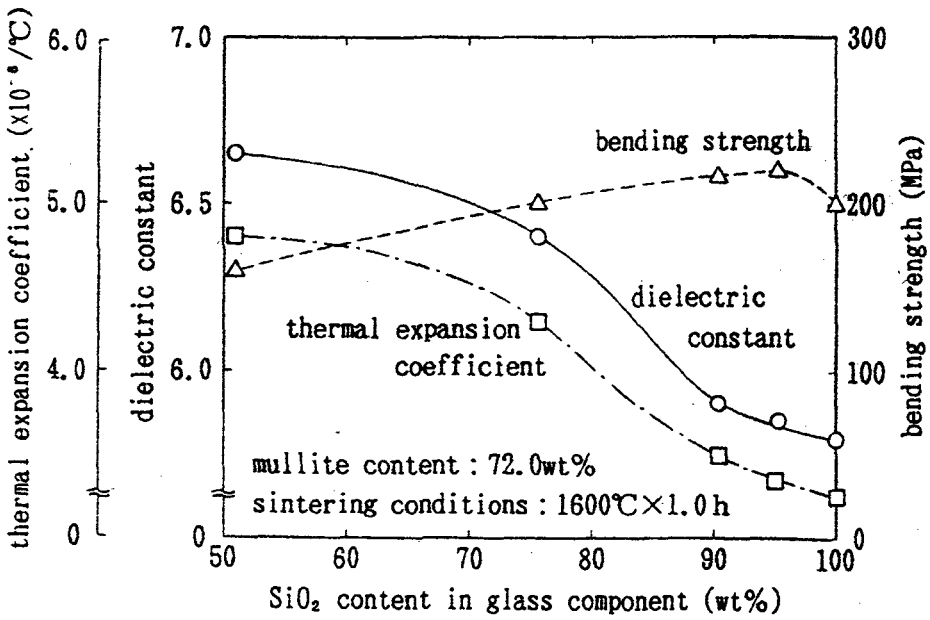


Figure 5 Effects of SiO_2 content on thermal expansion coefficient, dielectric constant and bending strength.[4]

3. Burn-out of organic binder at low temperature

Table 2[1] shows the performance features of the multilayer substrates for large comuters.

Table 2 Multilayer Ceramic Substrate Feature

	Hitachi[8]	Fujitsu[1]	NEC[1]	IBM[9]
Size(mm)	106×106×7	245×245×11	225×225×55	127.5×127.5
Wiring layer count	44	52	8	63
Wiring width (mm)	0.1	0.095	0.025	0.075
Input / output pin count	2521	8640	11540	2772
Shrinkage tolerance			<0.3%[10]	0.1%

These large substrates need to keep in high accurate dimension. During heating the burn-out gases from the organic binder should uniformely migrate from inside ceramic body to out.

Cofired substrates should keep the reducing atmosphere during firing to prevent the wiring metal oxidation. The 92-95% alumina substrates need the firing temperature of 1500-1600℃. However, the alumina-glass system are fired at the range of 800-1100℃. The burn-out of organic binder is difficult before the pore clossing of the ceramics in such low temperature firing. One of information was from Fujitsu[5] as shown in Figure 6. In this case,

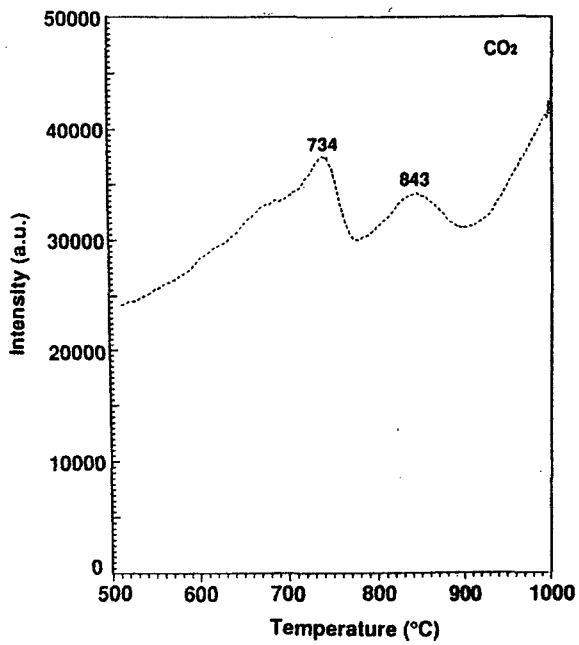


Figure 6 The relation between temperature and the intensity of CO_2 analysed by TG·DTG·MS method.[5]

back ground of measurement is at the 500℃ value. The carbonized binder needs to decompose at over 1000℃ in inert gas. Oxyzens of the carbon in final stage would originate from adsorpted water of the batch surface or reduced SiO_2 to SiO

If the decomposition of the binder is expected on the lower temperature, instead of the carbon oxidation, the main chain of polymer should partially consists the groups of -O-, -C=C-, -C(=O)- or such kind low binding energy chain

Table 3 is shown in the examples of the binders[6]. Poly-vinyl butylar has been recognized as the best material for tape casting process. However, this is one of difficult material for the burn-out. Polymeta acrylate is one of recommendable

Table 3 Typical Binder System for Tape Casting [6]

<Binder>	
Material Name	Structure
Cellose acetate	$[C_6H_7O_2(COOCH_3)_3]_n$
Poly acrylate	$(CH_2CHCOOH)_n$
Poly metaacrylate	$(CH_2CCH_3COOH)_n$
Poly binyl alcohol	$(CH_2CHOH)_n$
Poly binyl butyral	$[C_4H_8(CHOH_2)_2]_n$
<Plasticizer>	
Sucrose acetate isobutylate	$C_{12}H_{20}O_{11}CHCOC_4H_8O$
Glycerin	$C_3H_5(OH)_3$
Di-butyl phthalate	$C_6H_4(COO_2C_4H_9)_2$
Di-iso decyl phthalate	$C_6H_4(COOC_{10}H_{21})_2$

binder for low firing ceramics. If the residual carbon exists in the alumina-glass composite, the dielectric constant increases with increasing carbon content as shown in Figure 7[7]. Further more another difficulties

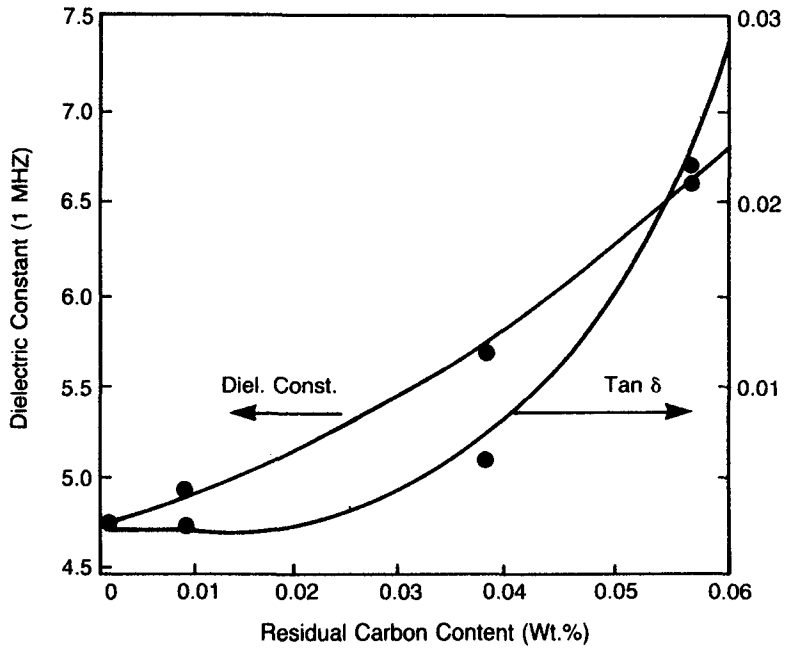


Fig.7. Electrical Properties vs. Carbon Content.[7]

encountered with the ceramic powder surface. Many polymers decompose at low temperature as shown in Figure 8[7]. When the polymer mixed with fine powdered ceramic batch used to form green sheets, the forms do not decompose similarly as shown in Figure 8[7] due to highly active chemical surface of the fine glass-ceramic powder.

All of these material batch is from refined reagents. For example, IBM is making the glass from the raw materials excepted Al_2O_3[11], then the glass is crashed to powder and sieved by a water flow siever to maintain the proper powder distribution. This is good for controlling surface chemical reaction.

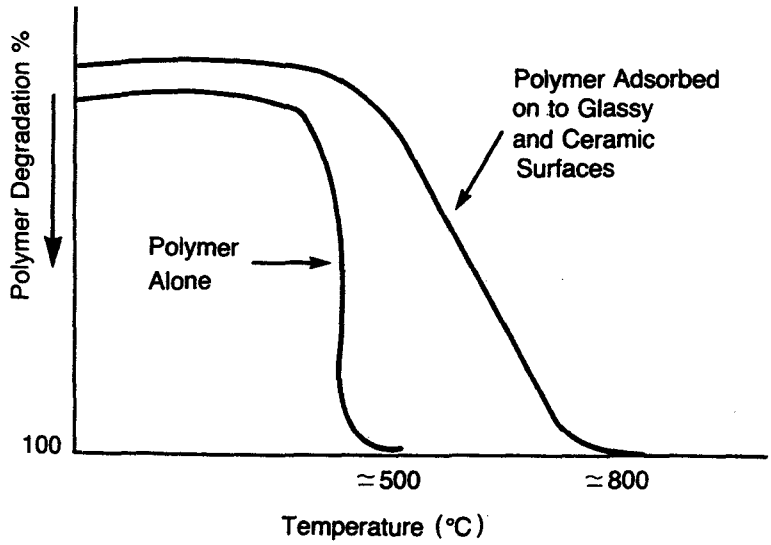


Fig. 8. Polymer Degradation on Ceramic Surfaces.[7]

Small amount of oxyzen is introduced to the forming gas such as H_2+N_2 for the decomposition of the residual carbon. This should be carefully controlled to prevent the wiring metal oxidation, thus thermodynamics of metal -O-C system should be considered as shown in Figure 9[7]

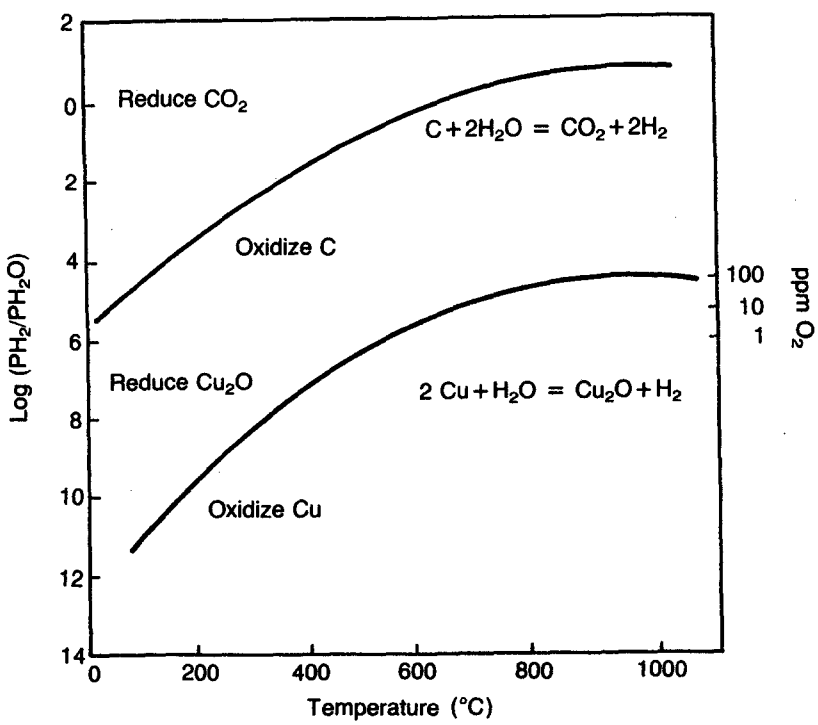


Fig. 9. Thermodynamics of Cu-O-C System.[7]

4. Improvement of mechanical strength

The bending strength of alumina ceramics is arround 300MPa. Typical glass ceramic of it is less than 100MPa without any improvement. Metallization induces some stress in the ceramic body, therefore over 200MPa of strength is prefferably required for the multilayer substrates. No information described in these papers listed Table 1 and 2, how to improve the bending strength. One paper[4] indicated the strength as shown in Figure 10 and 11.

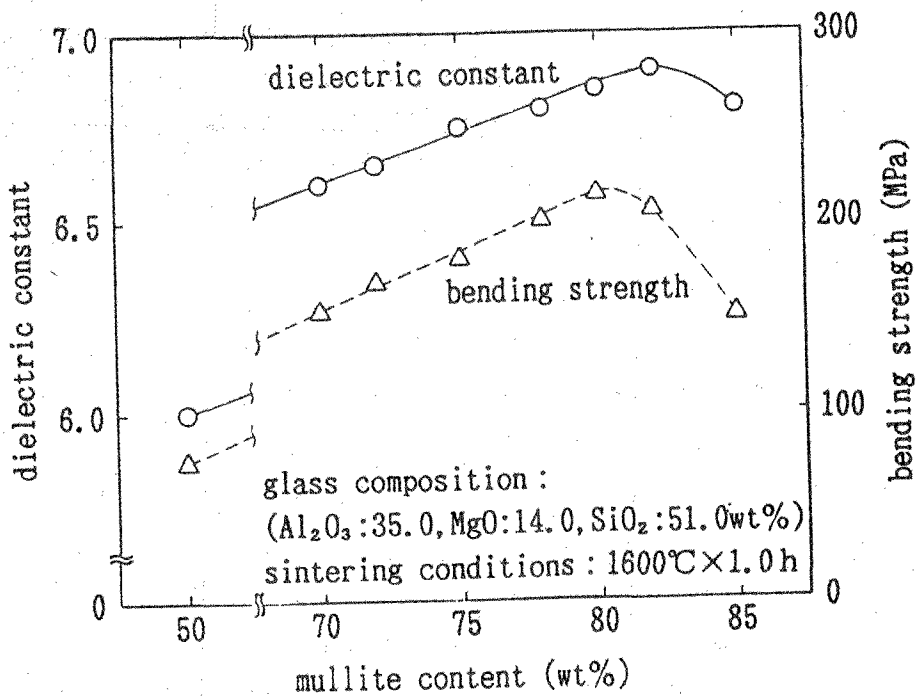
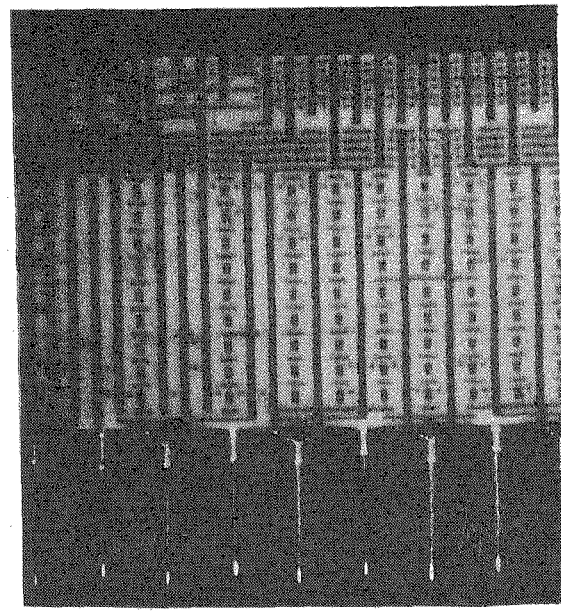


Figure10 Dependences of mullite content on dielectric constant and bending strength.[4]

Figure 11
Cross - section of Multilayer Ceramic Substrate[8)]



In Figure 10, providing over 200 MPa of the bending strength was in high content of mullite that is arround 80wt% of mullite. This made the high dielectric constant. The glass was partially replaced to silica glass that introduced to improve not only the bending strength but the dielectric constant. Master et, al,[7)] pointed out that the glass in the glass ceramic was cordierite crystallizable glass, thus provided the strong bending strength. Kamehara et, al,[3)] introduced that the sharp cornered voids in the glass-ceramic depressed the strength, thus approliate glass volume and firing temperature were required.

5. Preperation of multilayer ceramic substrate

Figure 12[12)] shows a typical preperation method for multilayer ceramic substrate. Recent process for the sophysticated substrates are similar as Figure 12, but tend to finner and precized technology. Figure 13 shows the cross section of the substrate[8)]. Each through-holes of the layers were laminated in fairly match their locations, that seemed as straight bars through the 44 layers.

Table 2 shows the firing shrinkage was controlled into as small as ± 0.1%, even if having 63 layers. Highest controlled value was realized by them in all sintering products which are affected by uncertain surface phenomena. Unfortunately, there are no information about how to. That is a limited technology, not an advanced technology which means the leading technology to affect other different field.

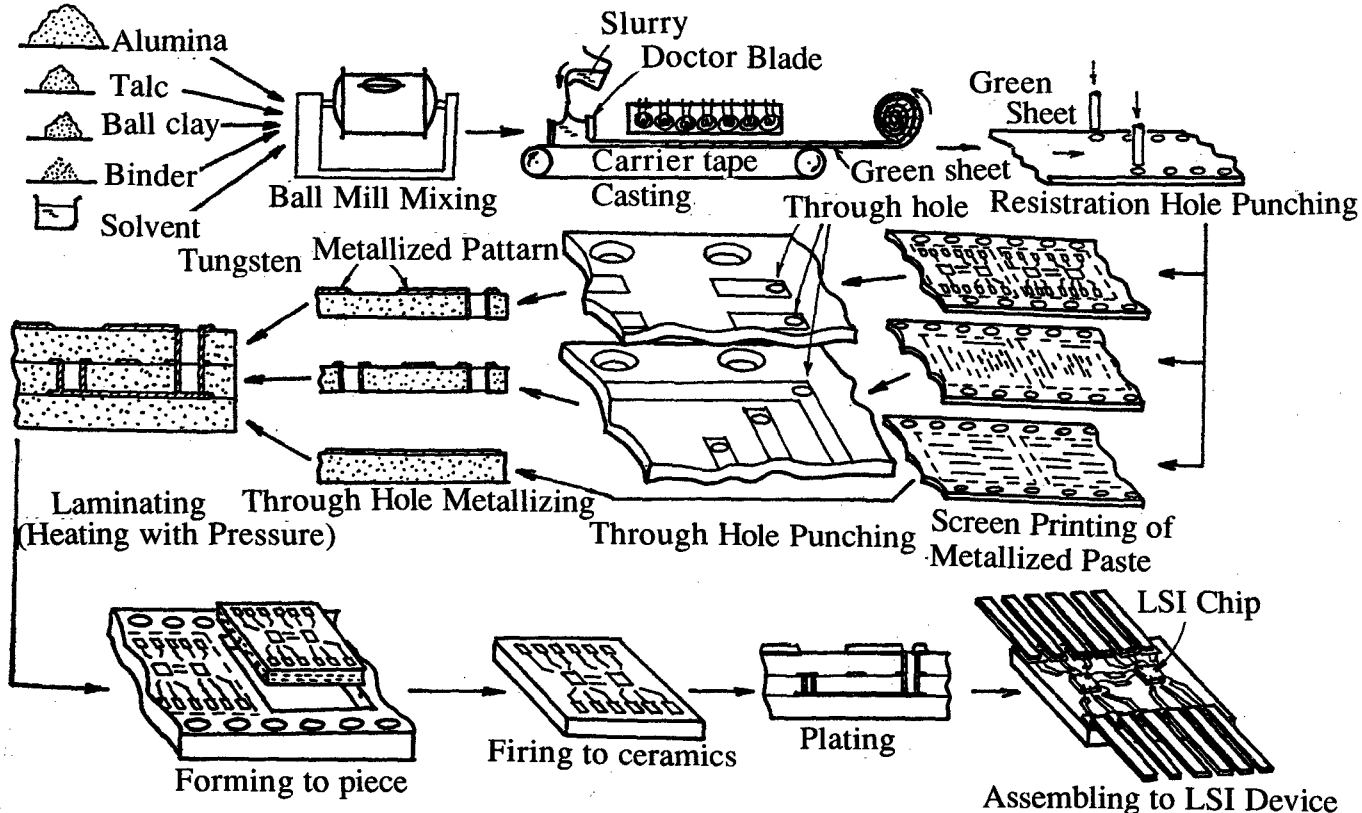


Figure 12 Production Process for Multilayer Package of LSI's [12]

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