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SHALLOW JUNCTION TECHNOLOGIES FOR FUTURE ULSI

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The formation of ultra-shallow junctions with depth less than 50 nm will be required in 0.1 μm CMOS and advanced bipolar devices. Various kinds of techniques, such as ion-implantation/rapid thermal annealing, low temperature epitaxy, rapid thermal diffusion and excimer laser doping have been developed to form shch ultra-shallow junctions. The advantages and limitations of these techniques are discussed. The perspective to ultra-shallow junction formation is also described.

1. INTRODUCTION

VLSI technologies toward smaller dimensions in device structure demand ever decreasing junction depths. The formation of ultra-shallow junctions is one of the key technologies in the development of the next generation VLSI.

For achieving ultra-shallow junctions, standard ion implantation technology is confronting with the difficulty such as the inherent channeling effect, damage, lateral diffusion under the mask and so on. In order to meet the requirement, various kinds of alternative technologies have been proposed. These are low-energy implantation with preamorphization, ultra-high vacuum low temperature epitaxy, gas-phase and solid state diffusion, and excimer laser doping.

In the practical use of these techniques, there are many fundamental issues to be discussed; process maturity, shallow junction capability, low leakage current density, low defect density, low sheet and contact resistance, ability to produce step-like profiles, ultra-high doping concenetrations and so on.

In the present paper, we discuss the advantages and limitations of each technique and show the perspective to shallow junction technology.

2. DEVICE REQUIREMENT

The schematic cross section of 0.1 μm p-channel MOSFET is shown in Fig. 1(a). In order to prevent short-channel effects, ultra-shallow pn junctions with depth less than 50 nm will be required for the source/drain formation when a gate length is reduced to 0.1 μm. Besides the surface carrier concentration of the source/drain regions must be sufficiently high to reduce parasric resistances.

The structure of advanced bipolar transistors is shown in Fig. 1(b). For very high speed performance, ultra-thin base width less than 50 nm will be required.

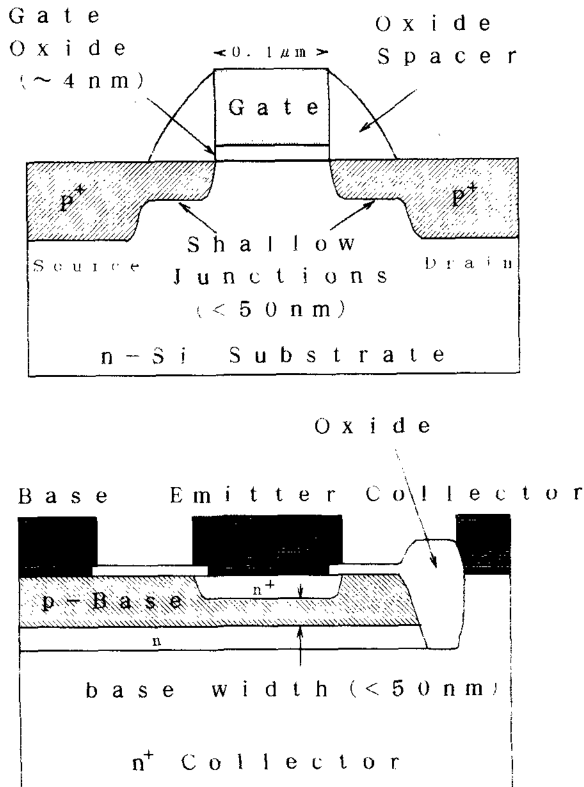

Figure 1. Schematic cross section of (a) 0.1 μm pMOSFET and (b) bipolar transistor.

3. SHALLOW JUNCTION TECHNOLOGIES

3.1. Ion implantation/rapid thermal annealing

Ion implantation technique has been used extensively for the fabrication of doped layers in silicon LSI. This technique can predict the implanted profiles precisely by controlling the ion dose and energy.

At low energy, the control of doping profiles, however, becomes difficult due to the ion-channeling. This problem is inherent in ion implantation for a single crystalline silicon. Channeling is particularly serious when a light ion like boron(mass 11), which is the only practical p-type dopant for silicon, is implanted at very low energy.

In order to eliminate channeling, amorphization of silicon prior to boron implantation (called as preamorphization) has been developed. However, it has been known that defects produced by preamorphization cause the anomalous diffusion. Using the experimental data by Miyake et al.[1], we analyze the anomalous diffusion quantitatively.

Diffusion coefficient of boron depends on the concentration itself when boron concentration exceeds the intrinsic carrier concentration at the diffusion temperature. It increases almost linearly with the concentration based on the model of the Fermi level effect[2].

The dashed curve in Fig. 2 shows the calculated profile, which was obtained by solving the diffusion equation including the above effect of the diffusion coefficient of D1 given in Fig. 3. It is obvious that the experimental plots (BF_2 15 KeV, $2x10^{15}cm^{-2}$ in preamorphized Si + 950 °C 15 s RTA) can not be modeled by only the concentration dependence of the diffusion coefficient. Much higher diffusion coefficient of D2 given in Fig. 3 is needed to explain the enhancement of the diffusion. This result indicates that much more silicon interstitials than thermal equilibrium , which were generated by the preamorphization process, exist at least in the boron diffusion region. Although preamorphization eliminates the channeling tail, it causes the generation of point defects like silicon interstitials, resulting the enhancement of the diffusion of boron. Thus, in the formation of ultra-shallow junctions, the above anomalous diffusion becomes a serious problem.

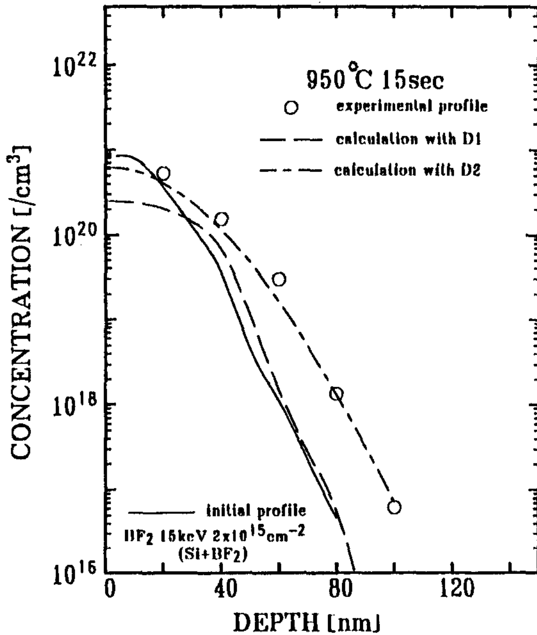

Figure 2. Experimental plots and calculated results of 950 °C, 15 s rapid thermal annealing of ion-implanted Si.

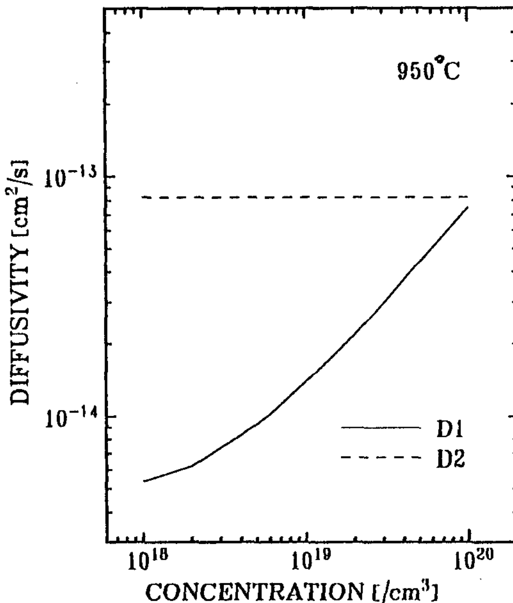

Figure 3. Diffusion coefficient of boron used in the calculation.

3.2. Low temperature epitaxy

High-quality epitaxial growth of silicon at temperatures as low as 550 °C has great potential for achieving the very-thin, abrupt doping profiles in LSI fabrication process. This technique can control the vertical doping profiles with the order of 10 Å. It has been reported [3] that low temperature epitaxial thin base was successfully used in Si or SiGe bipolar transistors and very high performance was attained.

However, many issues to be solved still remain. Selective deposition of silicon films, that is, growth on Si surface and non-growth on SiO_2 surface, is needed for fabrication of VLSI. At present, selective deposition by ultra-high vacuum low temperature epitaxy technique is limited by the spurious nucleation on the SiO_2 surface. Patterned wafer cleaning is also a key limitation. The control of defect density and leakage current for bipolar devices is still a challenging issue.

3.3. Rapid thermal diffusion

Thermal diffusion of impurities in silicon has been extensively studied from the early age of the device fabrication. There are many variations in the diffusion methods.

In recent diffusion technique, rapid thermal annealing (RTA) is mostly used for the incorporation of dopants. Here, we call it as rapid thermal diffusion. We discuss various kinds of rapid thermal diffusion briefly.

Ultra-shallow junctions were formed using gas-phase diffusion performed in the vertical CVD reactor operated at atmosphere pressure[4]. The boron atoms diffuse from the vapor-phase into silicon in hydrogen-diluted(0.1 %) B_2H_6. By varying the B_2H_6 flow rate, the surface boron concentration can be changed from 10^{19} to 10^{22} cm^{-3} as shown

in Fig. 4. However, the activation rate becomes fairly low at high boron concentrations and subsequent rapid thermal annealing is needed to activate boron concentration. Boron concentrations vary exponentially with depth as $\exp(-\alpha x)$, where x is the depth and α is a constant. Such profiles cannot be modeled by solving the diffusion equation under simple boundary conditions. The surface pre-cleaning becomes a problem. Furthermore, it seems difficult to form ultra-shallow junctions below 50 nm keeping with high surface carrier concentrations.

As a variation of solid-state diffusion, so called "molecular layer doping"[5] has been reported. In this method, adsorbed layers on the surface of silicon was formed by placing the wafer in the doping gas ambient of B_2H_6, which was used as a dopant source. Boron atoms were diffused by the rapid thermal annealing. This method can attain the very shallow junctions but has following problems. Mechanism of diffusion from the adsorbed layers by RTA is still not clear. No effective method for surface pre-cleaning is also a key limitation.

Diffusion technique from the doped oxide has been developed in the late '60s. The scheme of diffusion from the doped oxide is shown in Fig. 5. For short diffusion time, impurity concentrations in the silicon substrate are expressed approximately by the complementary error function(erfc) distributions. The surface concentration is determined by parameters of the dopant concentration in the oxide segregation coefficient at the interface between silicon and oxide and a ratio of diffusion coefficient in silicon and oxide.

By the combination with rapid thermal annealing, the formation of ultra-shallow junctions of 40 nm can be

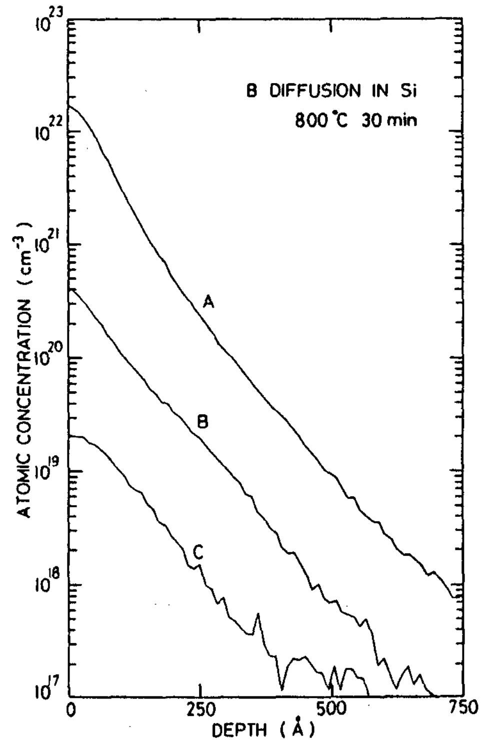

Figure 4. Boron concentration profiles obtained with different flow rate[4].

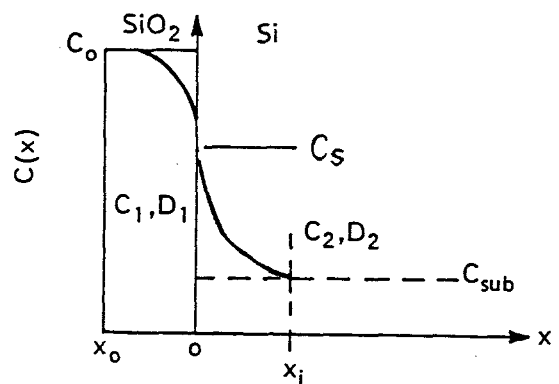

Figure 5. The scheme of diffusion from the doped oxide source.

attained as shown in Fig. 6[6]. The doping profile can be fitted well by the erfc distribution using a constant diffusion coefficient.

3.4. Excimer laser doping

A new doping technique using ultraviolet(UV) excimer lasers has been developed to form ultra-shallow junctions of dopants in silicon[7,8]. Silicon substrates are immersed with doping gases such as B_2H_6 and AsH_3 in the chamber during laser irradiation. The incident laser fluences cause the melting of silicon and simultaneously create dopant atoms by photolysis or pyrolysis of doping gas molecules. Then dopant atoms are incorporated into a molten region by the liquid-phase diffusion. UV excimer laser beam is absorbed extremely near the silicon surface because of a large absorption coefficient of silicon at UV regions, resulting in ultra-shallow junctions. The other advantage of laser doping is that very high carrier concentrations as high as $1\times10^{21}cm^{-3}$ exceeding solid solubility can be obtained by its non-equilibrium process.

Plots in Fig. 7 show the boron concentrations obtained by the "two-step doping"[9]. Two-step doping is a variation of laser doping, which consists of the two-step processes, i.e., deposition of boron films and melt of silicon. As shown in Fig. 8, high surface concentration ultra-shallow junctions can be obtained and experimental data are well fitted with Gaussian distributions. It has been reported [10] that p^+-n diodes with 30 nm junction depth are fabricated by laser doping and they exhibit ideality factors of 1.01-1.05 over 7 decades of current and reverse leakage current densities $10nA/cm^2$ at -5V reverse bias.

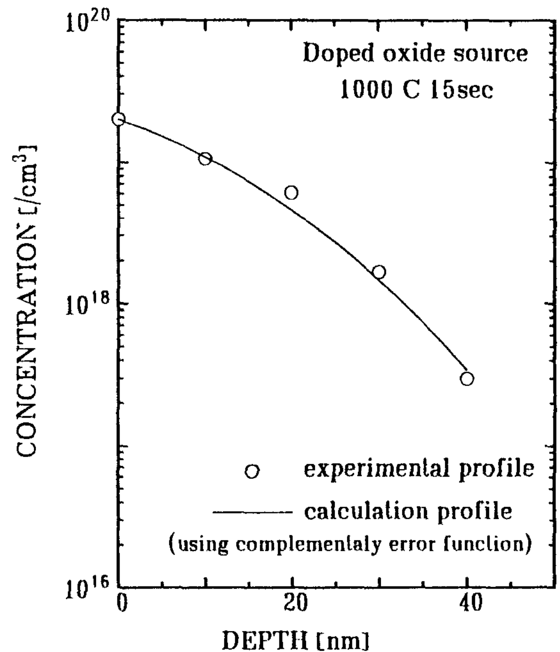

Figure 6. boron concentration profiles with the calculated result.

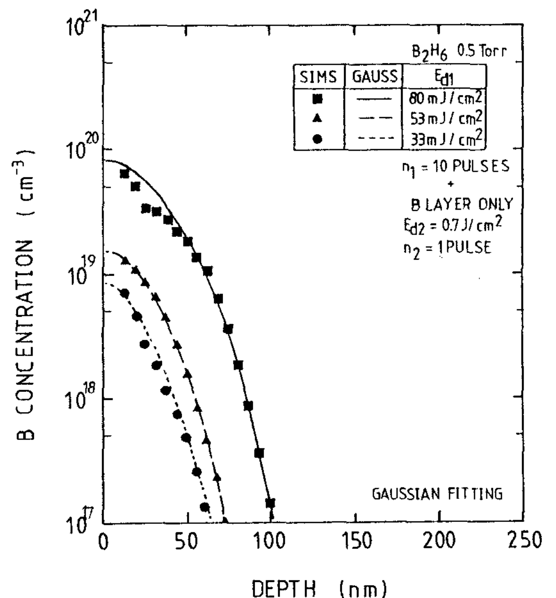

Figure 7. Boron concentration profiles and the calculated Gaussian distributions[10].

Table 1 Key advantages and limitations of each technology

	ADVANTAGES	LIMITATIONS
ION IMPLANTATION + RAPID THERMAL ANNEALING	equipment availability manufacturing data base process compatibility uniformity, reproducibility dose controllability	channeling anomalous diffusion damage annealing step for activation equipment modification
LOW TEMPERATURE EPITAXY	vertical profile control arbitrary dopant profile damage free	process compatibility defect density n-type difficult too complex
RAPID THERMAL DIFFUSION	damage free shallow junction process well characterized	profile tailoring(gas phase) high temperature process and dose control limited doping concentration
LASER DOPING	step-like doping profile low temperature process shallow junction	equipment availability process compatibility full wafer irradiation

4. SUMMARY

Various kinds of techniques forming ultra-shallow junctions are outlined. The advantages and limitations of ion implantation/rapid thermal annealing, low temperature epitaxy, rapid thermal diffusion and excimer laser doping are summarized in Table 1. The perspective to ultra-shallow junction is also described.

Acknowledgments

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