Advanced Materials '93, I / B: Magnetic, Fullerene, Dielectric, Ferroelectric,
Diamond and Related Materials, edited by M. Homma et al.
Trans. Mat. Res. Soc. Jpn., Volume 14B

MIGRATION PROBLEMS IN SUBMICRON METAL INTERCONNECTIONS

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Atom migration related phenomena due to a high current density and thermal and mechanical stresses have been serious reliability problems in submicron Al interconnects in ultra large scale integrated circuits. This paper shortly reviews present understandings of the mechanisms of a fatal void growth caused by these kinds of atom migrations. Various efforts to elongate interconnects life times such as alloying and strengthening by refractory metals, single crystallization, and usage of other low resistivity metals are also reviewed from a viewpoint of atom migrations.

1.INTRODUCTION

Various atom migration phenomena in submicron Al interconnections have been serious reliability problems in ULSI (ultra large scale integrated circuit). Stress induced migration which is caused by thermal and mechanical stress, and electromigration are especially important ones. There is a strong demand to improve reliability of interconnects since the shrinkage of interconnect dimensions progressed so rapidly. An enormous efforts have been paid to elongate a lifetime of interconnects such as alloying with Cu, Sc, and Ti, strengthening by combining with refractory metal layers, reducing gaseous contaminants which are introduced during sputtering. The advantages and disadvantages in these up-to-date technologies which strengthen traditional polycrystal Al interconnects are discussed in the following sections. Lastly, migration characteristics of newly proposed interconnect structures, Cu and single crystalline Al, will be reviewed.

2.ELECTROMIGRATION

Electromigration induced interconnects failures have been investigated from the early stage of Si technologies [1,2] . The empirical Black's formula of mean time to failure (MTF),

$$MTF = A \cdot J^{-n} \cdot \exp(Ea/kT) \qquad (1)$$

has been widely accepted [2]. In equation (1), A is a constant which depends on the interconnect structure, J is a current density, n is between 1.5 and 4 in most cases, and Ea is an activation energy which is usually between 0.4 and 0.7 eV corresponding to grain boundary activation energies. A typical scanning electron microscopy (SEM) observation of the failure caused by direct current (DC) stressing test is shown in Fig.1. A formation of a void at a grain boundary triple point, and a concomitant hillock formation at the anode side of the void is clearly observed. Most of failures are the line disconnections caused by a void growth, and short circuit failures sometimes occur also due to hillock and/or whisker growth [3]. It is considered that a void nucleation and growth is caused by a flux divergence of migrated atoms. An electromigration diffusion flux is formulated empirically as follows [4] :

$$\psi = (NDZ^{*} e \rho J / kT) \cdot \exp(-Ea / kT) \qquad (2)$$

where N is atom density, D is a constant, ρ is resistivity, and Z^{*} is an effective valence number which is negative value in most

cases. A diffusion flux at a grain boundary is several order of magnitudes larger than the lattice diffusion flux, since the activation energies Ea of grain boundary are 0.4 to 0.7 eV, which are much smaller than the lattice diffusion activation energy of 1.4 eV [5]. Thus, void formations are often observed at grain boundary triple points where a large flux divergence derived from grain boundary diffusion exists.

With a recent development of scale shrinkage, so-called " bamboo structure ", which grain boundaries are perpendicular to the interconnect longitudinal direction, have been realized in submicron width interconnects [6] (see Fig.2). The MTF of bamboo interconnects is several orders of magnitude longer than that of wide interconnects which consist of many triple points as shown in Fig.3 [7], and a large activation energy Ea around 1.0 eV has been observed [8].

3.STRESS-INDUCED MIGRATION

Interconnect open failures due to stress induced migration have been found for AlSi interconnects which were covered with SiO_2 films deposited by chemical vapor deposition (CVD) in the middle of 1980s [9,10]. The temperatures where open failures appear during the storage test are between 100 and 300 ℃. A typical SEM photograph of voids formed after CVD-SiO_2 film deposition and subsequent storage test is shown in Fig.4. A slit-like void and a wedge shape void are clearly formed at the bamboo grain boundaries. The existence of extremely large tensile residual stress in narrow interconnects have been verified by both computer simulated analysis [11] and direct stress measurements employing X-ray diffraction technics [12,13]. A change in stress during the thermal cycle test is shown in Fig.5 for both cases of a narrow interconnect and a film [12]. It is clearly observed that a hysteresis loop of the interconnect is very small as compared with that of the film. This means that the stress in Al interconnect cannot be relaxed due to the existence of overlayer SiO_2 film which adheres strongly to Al surface. Thus, the

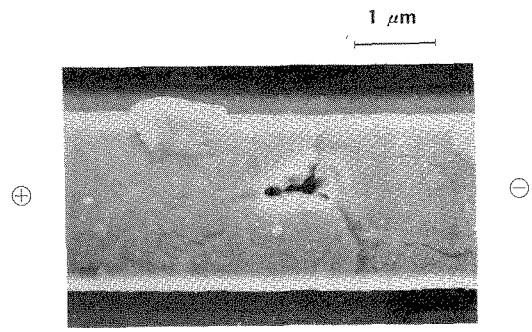

Fig.1 SEM observations of electromigration induced void and hillock formations.

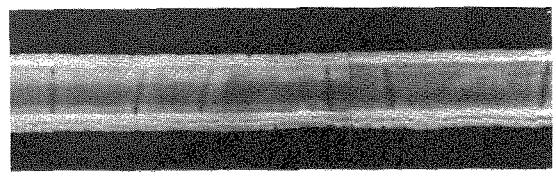

Fig.2 A bamboo-like interconnect formed after 400℃ annealing. A line width is 0.8 μm.

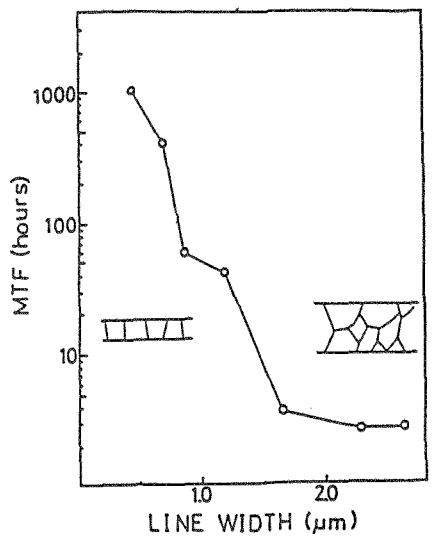

Fig.3 Line width dependence of electromigration MTF in AlSi interconnects. 200℃, $2x10^6 A/cm^2$.

stress relaxation takes place gradually during the storage test, and a void growth as a result of vacancy accumulation proceeds until open failure happens.

There have been lots of modelings of stress induced migrations [12,14,15,16]. Tezaki estimated stress relaxation rate as a function of temperatures by taking the

power law creep model into account, and qualitatively explained the existence of the temperature where the failure rate has the maximum. However, there have been a variety of failure modes which differs from each other, and a comprehensive modeling has not yet been established. For this reason, it has still been difficult to estimate MTF of stress-induced migration, and an accelerating test has not yet been established.

Another failure mode which takes place at temperatures higher than 400 ℃ has been reported [17]. Open failures are caused by the growth of wedge shaped voids in this mode, and an excellent in-situ observation of void formation and growth using HVTEM (high voltage transmission electron microscopy) was reported [17]. It is observed that initially a void is formed in the lattice and it grows into wedge shaped void at a grain boundary. It is not clear whether a stress in the interconnects is tensile at 400 ℃, and some other effect such as deformation and chemical-interaction of passivation film may relate to the void growth process.

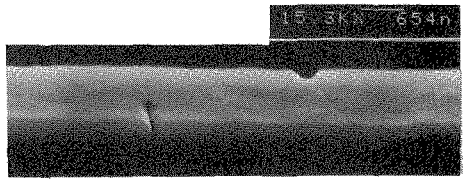

Fig.4 Voids formed after CVD-SiO_2 film deposition in AlSi interconnect.

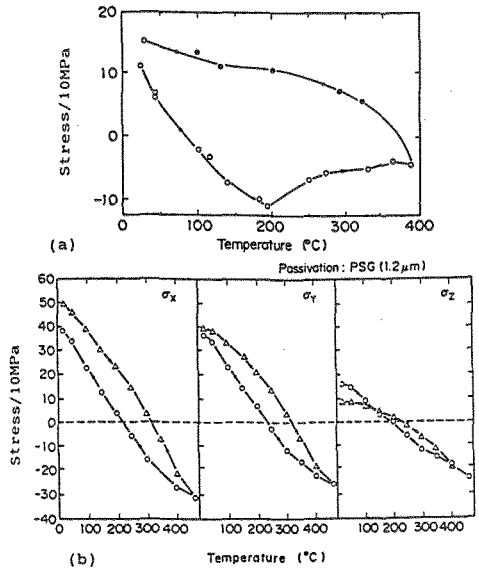

Fig.5 Stress-temperature curves measured by X-ray diffractions. (a) Al film, (b) Al interconnect covered by CVD PSG film. (from Ref. 12)

4. ALLOYING EFFECTS AND STRENGTHENING BY MULTI-LAYERED WITH REFRACTORY METALS

Effect of Cu addition for prolonging electromigration MTF has been known since 1970s [18,19], and it turned out that this was also effective for reducing failures due to stress induced migration [20]. The mechanisms are considered to be the grain boundary strengthening due to Cu-Al alloy formations at grain boundaries [21], and the reduction of vacancy diffusion flux due to coupling of vacancies with Cu impurities[20], and the lowering of the grain boundary energies. Addition of other metals such as Pd [22], Sc [23], have been reported effective. Mean Al grain size becomes small in most alloying cases. This is negative effect for electromigration, but positive for stress-induced migration since a yield strength increases with decreasing grain size according to Hall-Petch formula. However, it has been reported that both electromigration and stress-induced migration lifetimes improve in metals listed above. One typical example of a CuAl precipitate electromigration is shown in Fig.6 [24]. Movement of a precipitate into anode direction, and a concomitant void formation and movement into cathode direction at the cathode site of the precipitate are clearly observed. Electromigration drift velocity of Cu atoms is much faster than that of Al [25]. This causes mass depletion at the cathode side of the CuAl precipitate, which pronounces a void formation. It should be noted that too much addition of Cu causes substantial shortening of electromigration MTF in submicron width interconnects [24].

Al interconnects stacked with refractory metal layers have become main stream [26 - 29]. Even if a void acrosses an Al layer, the interconnect never disconnects since refractory metal layers still alive. Thus, stacked structures assure high reliability against stress-induced migration. Once a

large void is formed in the Al layer, a current density significantly increases in the refractory metal layers,and a resultant local heating enhances electromigration of Al near the void area. Enormously large hillocks or whiskers, which cause short circuit failures, can be formed by this mechanism as shown in Fig.7. Thus, it is a key issue to suppress electromigration of Al layers in multilayered structures. For this purpose, grain size enlargement due to annealing stress by the top-layer CVD-W film [27], and continuous interface formation between underlayer TiN and Al [29] have been reported. When Al is deposited successively on (111) aligned TiN,

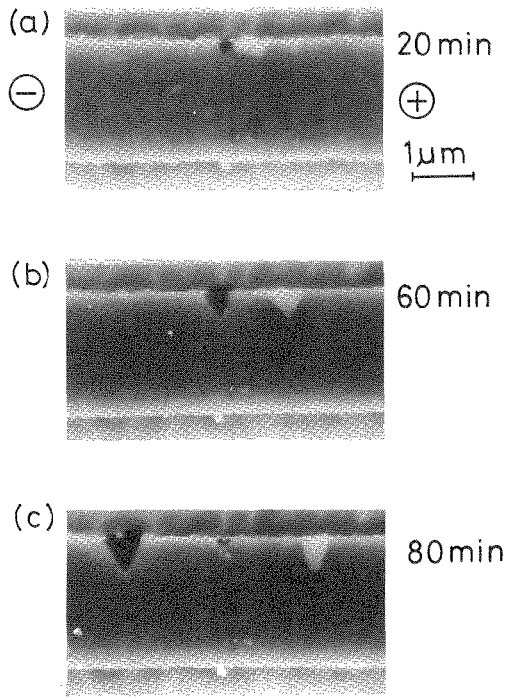

Fig.6 Electromigration behaviors of a CuAl precipitate (bright one), and a void (dark one).

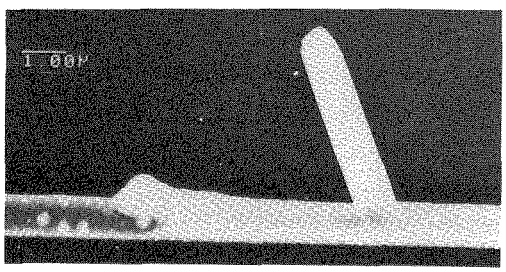

Fig.7 A large whisker formed due to DC current stress test in AlSi/TiN/Ti multi-layered interconnect.

highly (111) aligned Al interconnects are formed and prolongation of electromigration MTF has been observed.

There is a close relationship in fabrication processes between via/contact hole technologies and Al multilayered interconnect technologies. Recently, void formations at the interface between Al and refractory metals in via/contact holes have been reported [30,31]. Since there are significant differences in electromigration atom flux between Al and refractory metals, this failure occurs intrinsically. Some geometrical improvements which avoid severe current concentration at the interface would be desirable.

5. CU INTERCONNECTS, AND SINGLE CRYSTALLINE AL INTERCONNECTS

Two directions for developing the next generation interconnects have been recognized recently. The one is Cu interconnects [32,33] and the other is single crystalline Al interconnects [34,35]. Cu has excellent properties such as a low electrical resistivity and a higher melting temperature than Al, which means a low self-diffusion constant due to a high activation energy. However, many other difficulties in fabrication processes exists. Difficulty in dry etching due to a high vapor pressure, high diffusion constant, poor adhesion on SiO_2, and high chemical reactivity with oxygen and other materials. Lots of papers have been reported which showed the excellent electromigration reliability of Cu interconnects as compared with Al [32,33,36,37]. However, MTF data distributed widely depending on the fabricating conditions. On the other hand, there has been only one report on stress-induced migration properties [38], which showed frequent void formations due to CVD-SiO_2 film deposition. This may relates to high diffusivities of Cu in Si and SiO_2, and hence, it is necessary to encapsulate Cu interconnects by diffusion barrier layers such as refractory metals or SiN [37,39]. It is strongly desired to get basic metallurgical understandings of Cu interconnects such as grain growth behaviors, stress relaxation characteristics, and alloying effects.

A single crystalline Al is one on the most reliable interconnect materials which have ever been reported [35]. A comparison of electromigration MTF between single crystalline Al and polycrystalline Cu is shown in Fig.8 [35]. It is shown that a single crystalline Al has more than 2 order of magnitude longer MTF than polycrystalline Cu. After the severe accelerating test of 3100 hours, a large void which was surrounded by (111) planes was formed at the cathode electrode as shown in Fig.9. This void was formed due to coalescence of small voids which moved from the anode direction.

Typical characteristics of single crystalline Al are the shape of voids which are surrounded by low energy crystal planes. Chamfer like voids is formed when an interconnect id parallel to (110) direction [34]; this behavior assures an extremely high resistance against stress-induced open circuit failures. It should be noted that a single crystalline film has a very low yield stress.,Although a void is easily formed in single crystalline interconnects, a fatal slit-like void growth is completely suppressed [16]. A very simple in-situ annealing method for making single crystalline interconnection on SiO_2 has been proposed [40]. The possibility of practical application depends on how large area can be single-crystallized. A further breakthrough relates to fundamental understanding of interfacial energy effect on grain growth may be needed.

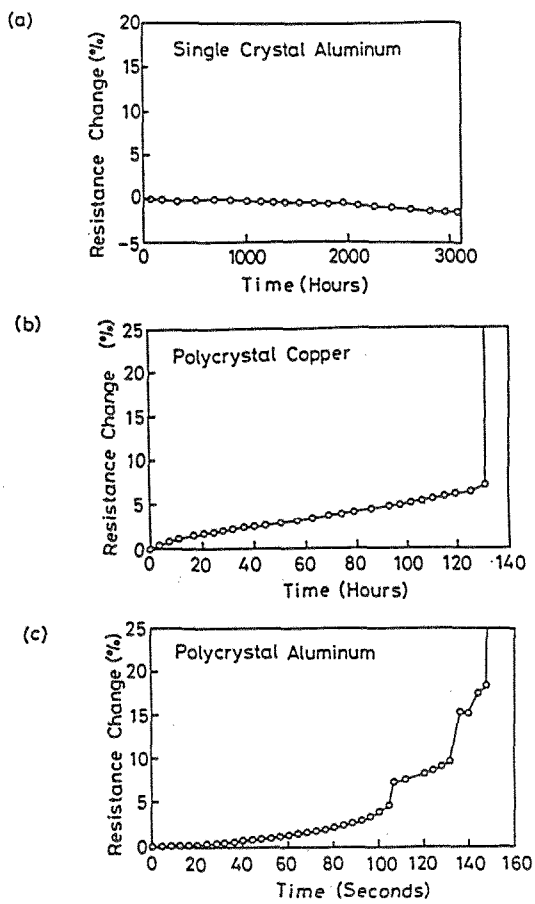

Fig.8 Resistance changes for various interconnects during DC current stress test. 150℃,1x10^{7}A/cm^2.

6.CONCLUSIONS

The goal for the highly reliable polycrystal interconects has not been clear, although the alloying effects and the control of crystal orientations into highly (111) or (100) aligned structures [16] are believed to be essential at present. There are also many difficulties to make a single crystalline interconnects in practically applicable levels. In both ways, precise control of grain growth and crystal orientations by deposition and /or annealing methods are key issues. The deep understandings of the roles of impurity species at grain boundaries and interfaces for the complex behaviors of voids are essential to obtain designing principles. Molecular dynamics simulations [41] and in-situ observations using TEM [18] and SEM [42], scanning μ-RHEED [43], and STM/AFM would be powerful tools for this purposes.

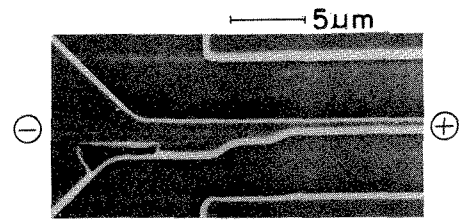

Fig.9 A void formed at the cathode electrode after 3100h accerelating test in a single crystalline Al interconnect.

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