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SILICON-ON-DIAMOND FIELD EFFECT DEVICES

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On a 4" silicon wafer a heavily doped B/Ge epi layer followed by an undoped epi layer were deposited. On this substrate a CVD diamond was deposited and this wafer was bonded to another silicon wafer with a thin polysilicon buffer layer. The starting substrate and the etch stop layer were removed to obtain a silicon-on-diamond structure. Characteristics of MOSFET devices built on such a structure is presented.

1.INTRODUCTION

Silicon-on-diamond (SOD) is a form of silicon-on-insulator (SOI) technology. In addition to the various advantages claimed by SOI, the Silicon-on-diamond technology has the following additional characteristics: (1) Diamond being a good thermal conductor will permit device dimensions to shrink thereby enabling ULSI circuits development (2) Diamond is a radiation hardened material because of its tight bond. In order to develop an SOD device technology it is necessary that the diamond is a very good electrical insulator. Further the requirements for bonding of CVD diamond deposited silicon wafer to another silicon wafer should also be considered. There are a number of schemes[1,2] to fabricate an SOD structure, but here we will discuss only about Bond and Etch Back Silicon-On-Diamond (BESOD) structure. Bond and etch back scheme is being very successfully used in SOI technology[3].

2.BESOD STRUCTURE

The sequence of fabrication steps for forming a BESOD[4] is shown in Figure 1. Two epitaxial layers are grown on a seed silicon wafer (1): The first layer (2) is an etch stop layer with a heavy doping of boron and germanium, the second layer (3) is an undoped silicon layer of desired thickness to fabricate the desired devices. A CVD diamond film[5,6](4) of about 1.5 μm is deposited[7] on top of the undoped Si epi layer (3). On top of the diamond film (4), a 10 μm or so thick polysilicon (5) is deposited and polished to obtain a smooth surface. A standard

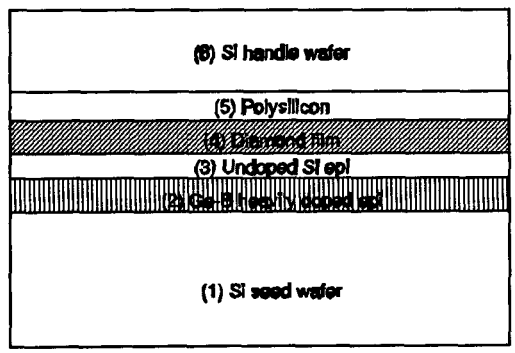

Figure 1 Scheme to form SOD structure.

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silicon wafer (6) is bonded to the polysilicon layer. we will discuss about bonding later in this section. Now the wafer is turned around, and the seed wafer (1) and etch stop layer (2) are removed by grinding and chemical etching to obtain a silicon-on-diamond structure. A polysilicon layer is necessary to bond two wafers together due to the roughness of the diamond film. Bonding of the wafers are accomplished by placing two wafers in intimate contact at 800° C for 10 minutes in N_2 ambient. Even though bonding is between two silicon surfaces, actually bonding takes place between the two native oxides.

The diamond surface, if it is very smooth, can be bonded directly onto a silicon wafer. All substrates had quite a rough surface and hence a polysilicon buffer layer was essential to effectively bond the two wafers. The polysilicon buffer layer was polished to obtain a very smooth surface to enhance the bond. The hydrogen is believed to bridge the gap between the two wafers where ever they are not in good intimate contact. At elevated bonding temperature, OH^- groups are believed to disassociate and thus available oxygen molecules react with silicon to form SiO_2 and this oxide fills the gaps between the two wafers.

Most of the seed wafer was removed through grinding with a wafer grinder. Two chemical etches were used to remove the remaining handle wafer and the etch stop layer. An EPW (ethylenediamine-pyrocatechol-water) was used to remove the remaining handle wafer up to the etch stop layer. The etchant to remove etch stop layer is 1 part HF (49%), 3 part HNO_3 (70%), and 8 parts CH_3COOH. The residual layer at the end of etch stop layer is removed by a non-selective etch.

3.BESOD MOSFET's

A number of discrete MOSFET's were fabricated on the overlayer silicon on top of the diamond film. For comparison, few of the SIMOX wafers were used for device fabrication subjected to the same type of processing steps. The fabrication process sequence for BESOD MOSFET's are shown below:

1. Mesa formation by photolithography, reactive ion etch and resist removal
2. RCA clean and 80 nm PECVD oxide deposition and annealing at 800° C in N_2 for 30 min
3. Deposition of in situ n-type polysilicon and gate electrode formation by photolithography, reactive ion etch and resist removal
4. Definition of NMOS Source/Drain areas and Ion Implantation of Source/Drain and resist removal
5. Deposition of 500 nm PECVD oxide and contact formation by lithography, ion etch and resist removal.
6. Annealing at 800° C for 30 min in N_2
7. Contact etching and metallization of Al/Si/Cu
8. Sintering at 425° C for 30 minutes in N_2

4.BESOD MOSFET CHARACTERISTICS

The subthreshold (I_D - V_G) characteristics of a BESOD NMOS FET is shown in Figure 2. Both

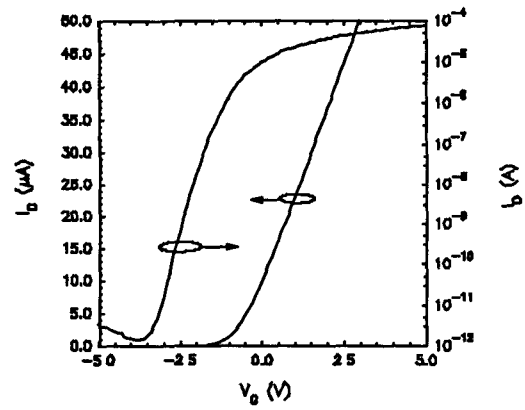

Figure 2 Subthreshold characteristics for BESOD NMOS FET.

the linear and semilog I_D characteristics as a function of V_G are shown. The current variation is about eight orders of magnitude from off to on state. The I_D - V_D characteristic curves as a function of gate voltage for the above device is shown in Figure 3. The linear and saturation characteristics are normal like any other MOSFET device. The following parameters are obtained for this device: V_T = -0.7 V, g_m = 13.7 μS, Subthreshold swing, S = 0.295 V/dec. The threshold voltage varied from +3.7 V to -0.6 V. The g_m value varied from 2 to 13.7 μS, and S varied from 0.5 to 1.2 V/dec. Considering that it is the very first try to

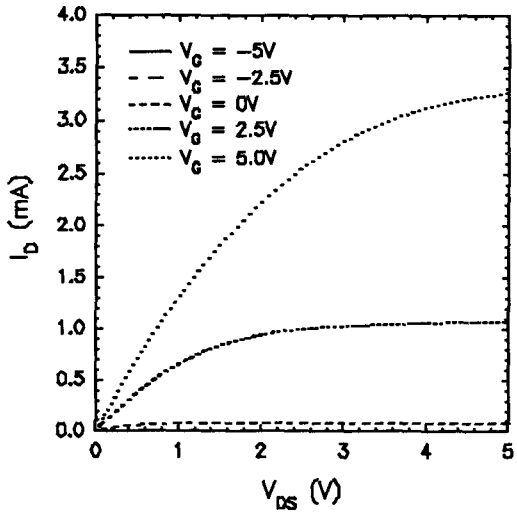

Figure 3 I_D-V_D characteristics for BESOD NMOS FET.

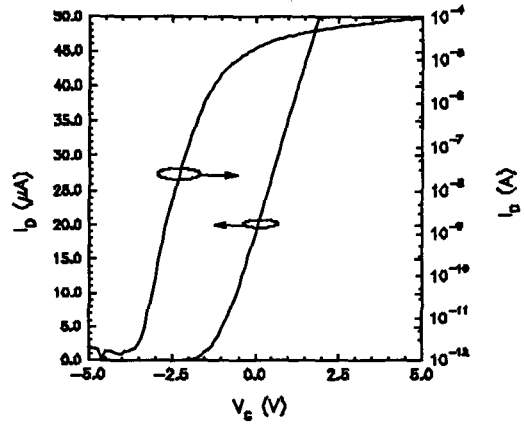

Figure 4 Subthreshold characteristics for SIMOX NMOS FET.

fabricate devices on BESOD substrate the results are very encouraging. The doping was not optimized for threshold voltage adjustment. There was some spread in both g_m and S values. The diamond film thickness non uniformity is a problem. The interface between diamond and silicon is not the same as between silicon dioxide and silicon. The diamond resistivity of buried diamond was not uniformly high compared to the buried silicon dioxide. The leakage current through diamond was of the order of 100 to 150 pA during the subthreshold measurements.

The subthreshold characteristics of a SIMOX NMOS FET of a simultaneously fabricated device is shown in Figure 4. The characteristics are very similar to the ones we see in Figure 2. The I_D - V_D characteristics for various gate voltages are shown in Figure 5. The following parameters were obtained from the above characteristic curves for the SIMOX device: V_T = -1.2 V, g_m = 16.3 μS, and S = 0.25 V/decade. The threshold voltage for the SIMOX devices varied from -1.1 to -1.2 V. The g_m varied from 15.1 to 16.5 μS, and S varied from 0.29 to 0.31 V/decade. The variation of various device parameters in the case of SIMOX was considerably small compared to the BESOD devices. The buried oxide thickness is much more uniform compared to the diamond film thickness. Further the electrical resistivity of the buried diamond film is not as high as the implanted buried oxide. Hence considerable improvement in the electrical resistivity and the thickness uniformity of the diamond film is very essential for this technology to become viable.

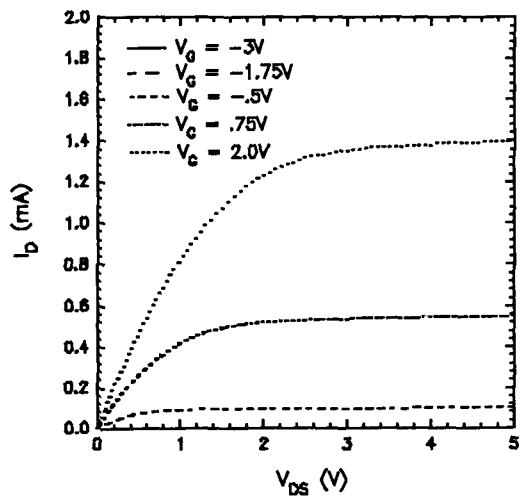

Figure 5 I_D-V_D characteristics for SIMOX NMOS FET.

The current-voltage characteristics of the capacitor structure fabricated on the same chip as the MOSFET's were studied. From this measurement the J-E and ρ-E characteristics of the capacitor were

computed. These J-E and ρ-E characteristics plots are shown in Figure 6. The leakage current flowing through the diamond film was measured and the current density was computed knowing the area of the capacitor dot. The capacitor area was somewhat large (7×10^{-3} cm^2). The voltage during this test was varied from 10^{-2} V to 10^3 V. The resistivity of the diamond was rather low at low to moderate fields and further decreased rapidly at very high fields. The resistitivity was about 10^8 Ω-cm at the operating voltages of the MOSFET. The resistivity of the SIMOX capacitors were nearly constant at 1×10^{12} Ω-cm even up to 10^6 V/cm.

5.DISCUSSION

This is the first report on devices fabricated on a BESOD structure. As mentioned earlier the diamond resistivity and surface morphologies were major factors in yielding devices having good device parameters. We are in the process of making improvements in the diamond film electrical resistivity and surface morphology. Devices on SOD structure is similar in performance to simultaneously fabricated SIMOX devices even though the diamond resistivity was four orders magnitude low compared to SIMOX. Interface between silicon and diamond is far different from the interface between silicon and silicon dioxide.

6.CONCLUSION

We have been successful in bonding a diamond deposited silicon wafer to a silicon wafer by having a polysilicon buffer layer, in etching back to form an SOD structure, and in fabricating MOSFET devices in such a structure. The results are encouraging and we hope to make progress in this technology. The quality of the CVD diamond deposition needs improvement in terms of the its electrical resistivity, and surface morphology. This diamond film quality improvement will help us in bonding the diamond film deposited silicon wafer to a standard silicon wafer without the polysilicon buffer layer. The improvement in the diamond quality and bonding process should yield high performance devices and thereby yielding the BESOD technology as a viable technology for high temperature and radiation hardened applications.

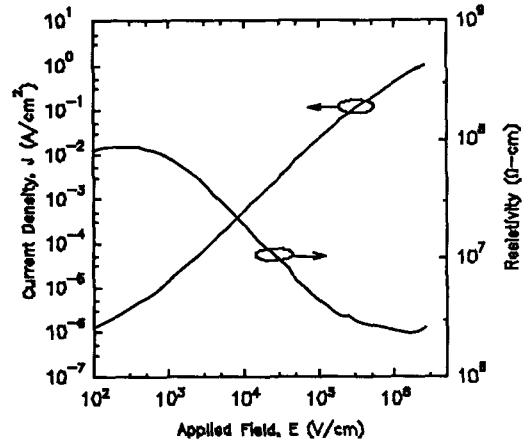

Figure 6 Current density and resistivity for buried diamond layer.

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