Advanced Materials '93, I / B: Magnetic, Fullerene, Dielectric, Ferroelectric,
Diamond and Related Materials, edited by M. Homma et al.
Trans. Mat. Res. Soc. Jpn., Volume 14B

Metal CVD technology

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Selective chemical vapor deposition of metal has an excellent potential for the multilevel metalization of ultra-large scale integrated circuits. In this article, we describe the recent progress of the selective Al growth technology using dimethylaluminum hydride [DMAH, $(CH_3)_2AlH$]. It has been found that, by thermal decomposition, 0.3μm-diam./1μm-deep SiO_2-via-holes on Si surface are filled with the selective single-crystal Al. The as-grown CVD-Al/n^+-Si contact has the low contact resistivity of $2x10^{-7}\Omega cm^2$. Furthermore, the erosion has not been observed at the CVD-Al/Si interface after the annealing at 450°C/N_2/30min. We have recently proposed a new MOSFET structure; Self-Aligned Selectively-deposited-Al (SAL^2) MOSFET. In SAL^2-MOSFET, the sheet resistance of the poly-Si gate and the source/drain regions as well as the contact resistance are dramatically reduced.

1. INTRODUCTION

Deep submicron multilevel metalization is indispensably required in ultra large scale integrated (ULSI) circuits. Aluminum and Al alloys are still choice interconnect materials. Chemical vapor deposition (CVD) of Al has been investigated for its capability of achieving conformal step coverage, selective growth onto the electrically conductive surface, and single crystal growth on the Si wafer. The selective deposition is the most distinguishable feature of CVD technology [1-3]. Furthermore, the selective and the subsequent nonselective deposition of Al is the most promising for the planarization of deep-submicron via holes. However, the Al CVD technologies are not yet suitable for practical use, because they do not provide full control of selective and nonselective deposition of high quality Al.

We have developed selective CVD technology of single crystal Al using dimethylaluminum hydride [DMAH: $(CH_3)_2AlH$] and H_2 [4-8]. Filling capability to deep submicron via holes and the complete planarization by the selective and the subsequent nonselective deposition have been demonstrated. We have proposed a new MOSFET structure in which the poly-Si gate electrode and the source/drain regions are covered with the selectively deposited Al, resulting in the dramatic reduction of the parasitic resistance of MOSFET. As a selective growth mechanism, we have proposed and experimentally confirmed a surface electrochemical reaction model, where surface free electrons catalytically contribute to the surface reaction [6-8]. Based on the surface electrochemical reaction model, we have proposed a new atomic resist process [9,10]. In this atomic resist process, the monolayer hydrogen terminated on the Si surface, and the atomic resist is patterned by an electron beam lithographic technique. Then the patterned Al is selectively deposited on the H-terminated surface by the selective Al CVD using DMAH and H_2. The Al CVD technology also has a potential for fabricating nanometer dots and lines in the future atomic-scale devices.

In this paper, we review our recent progress of selective Al CVD technology, emphasizing the application to ULSI.

2. SELECTIVE Al GROWTH

2.1 Selective Al growth on Si

Aluminum was deposited by low-pressure

CVD using dimethylaluminum hydride [DMAH; $(CH_3)_2AlH$] and H_2. The DMAH used was a clear viscous liquid and had a vapor pressure of 2 Torr (20°C), which was ten times higher than that of triisobuthylaluminum. The DMAH and the H_2 carrier gas were introduced into a horn-type quartz reactor. A 4-in.-diam. Si wafer was placed on a heated susceptor.

Plain Si wafers and SiO_2-patterned Si wafers were chemically cleaned by H_2SO_4:H_2O_2 (4:1) solution with an intermediate rinse in ultrapure water. The wafers were then pretreated just before Al deposition by a short dip in HF:H_2O (1:50 - 1:100) solution in order to remove residual oxide on Si surface, followed by an ultrapure water rinse. The typical rinsing time was 10min. After the above cleaning, the cleaned Si surface is mainly terminated by hydrogen [11]. The terminated hydrogen plays an important role in the selective growth of Al on Si and in the atomic hydrogen resist process [6-10].

Aluminum films were deposited at a total pressure of 1.2-3.0 Torr and a partial pressure of DMAH of $(3-7)\times10^{-3}$ Torr. The deposition rate (DR) on Si was found to have a surface reaction limited form: $DR=DR_0\exp(-E/kT)$, where E=0.3eV in the temperature range of 230-350°C. The typical deposition temperature was 270°C and the

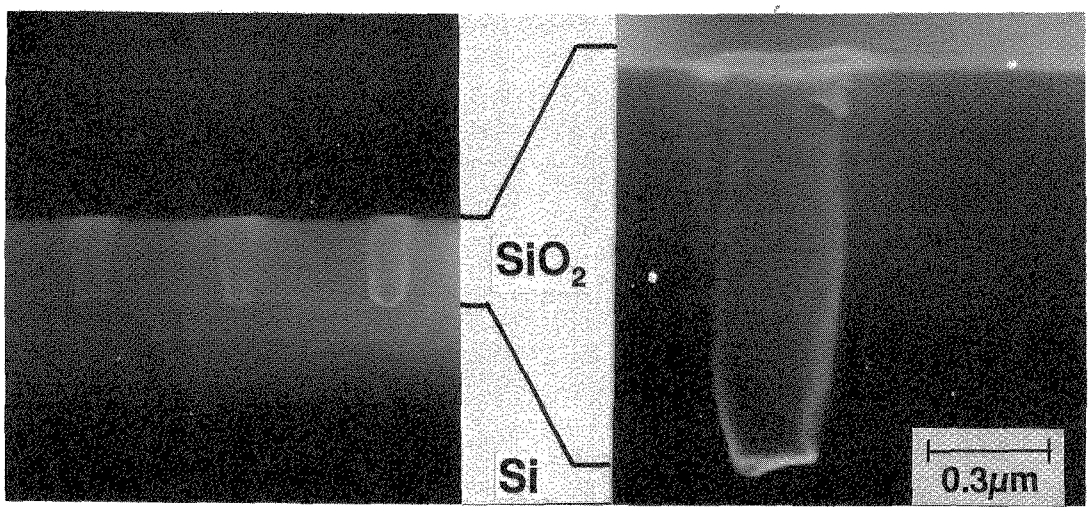

Fig. 1. SEM micrographs of selectively deposited Al into deep-submicron via-holes.

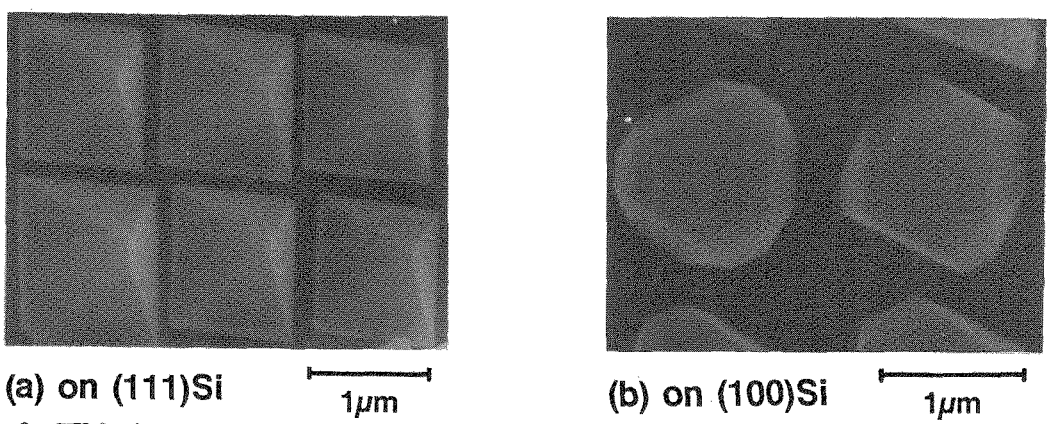

Fig. 2. SEM micrographs of overgrown aluminum. (a)via holes on (111)Si, and (b) via holes on (100)Si. The diameter and depth of the via holes are 0.8μm and 1μm, respectively.

typical deposition rate was about 800Å/min selectively into via holes on Si. The electron spectroscopy for chemical analysis (ESCA) revealed that carbon and oxygen were absent from the bulk of the film. Since carbon was not incorporated in the deposited Al film, the total reaction to produce Al from DMAH and H_2 was considered to be

$$(CH_3)_2AlH + \frac{1}{2} H_2 \rightarrow Al \downarrow + 2CH_4 \uparrow.$$

The resistivity of Al film was 3μΩcm, which was very close to the bulk resistivity of 2.65μΩcm.

Figure 1 shows the selectively deposited Al into deep-submicron via holes [6]. The diameter and depth were 0.3μm and 1μm, respectively, and the aspect ratio was larger than 3. Furthermore, 0.18μmϕ/0.4μm-deep via holes has been filled with the selective Al.

Figures 2(a) and 2(b) show selectively deposited Al into SiO_2 via holes on (111) Si and (100) Si, respectively. Diameter and depth of via holes were 0.8μm and 1μm, respectively. The Al was selectively overgrown after filling the via holes. The overgrown Al exhibited a pyramidal shape for via holes on (111) Si and a triangular terrace for those on (100) Si. By determining their own shapes of single crystal planes of Al, it can be immediately confirmed that the single crystal (100)Al and (111)Al are selectively deposited on (111) Si and (100) Si, respectively [5]. The single crystal structure of the CVD Al has been also confirmed by the observation of reflection high-energy electron diffraction (RHEED) patterns and the newly developed scanning μ-RHEED microscope [12,13]. The crystallographic orientation of single crystal (100)Al on (111)Si was determined to be <011>Al/<112>Si and <011>Al/<110>Si from the simultaneous RHEED pattern observation of Al and Si substrate [14].

Aluminum deposition on various surface has been investigated. It has been found that Al is deposited on electrically conductive materials such as n-Si, p-Si, Ti, TiN, Ti-silicide. On the other hand, the Al is not deposited on the electrically insulating materials such as thermally oxidized SiO_2, CVD SiO_2, phosphosilicate glass (PSG) and borophosphosilicate glass (BPSG).

2.2 Complete planarization of via hole

The selective and nonselective growth is necessary for planarizing via holes, *i.e.*, the growth mode should be continuously changed from the selective to the nonselective one.

We have developed a plasma excitation technique to change the deposition mode from the selective to the nonselective mode [5,7]. Via holes have been planarized by the selective and the subsequent nonselective growth of Al as shown in Fig. 3. The planarization procedure was as follows: at first, Al was deposited selectively on Si surface by thermal decomposition. Just after the via hole filling, the rf(13.56MHz)-excited plasma was generated in a quartz reactor for 1min. The rf plasma was generated using the three-separated ring electrode. After the above 1 min, the Al film was deposited nonselectively on the SiO_2 surface as well as on the selectively deposited Al, because a very thin Al layer was formed on the insulating surface during the plasma excitation duration. Thus, the SiO_2 via holes were completely planarized. It has been confirmed that the supply of free electrons mainly contribute to the nonselective deposition of Al onto the insulating surface from the measurement of the electron temperature and the electron density [7].

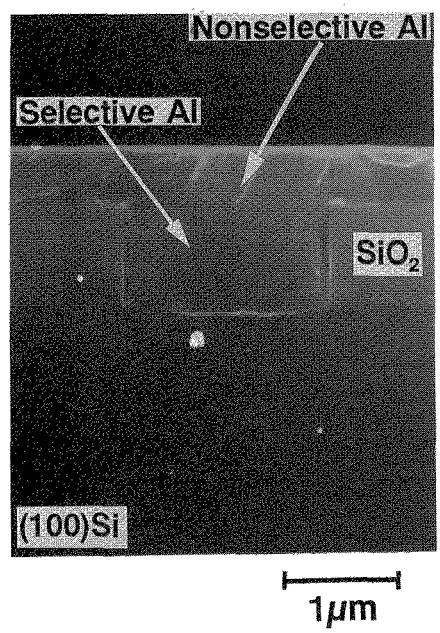

Fig. 3.
Complete planarization of via holes with the selective and the subsequent nonselective Al.

3. CONTACT CHARACTERISTICS OF CVD-Al/Si INTERFACE

Figure 4 shows the contact resistance of as-deposited CVD-Al/n^+-Si as a function of contact size. The specific contact resistivity of as-deposited Al/n^+-Si contact was found to be as low as less than $2\times10^{-7}\Omega cm^2$ [6]. This value is less than 1/5 - 1/10 of the conventional Al-Si/n^+-Si contact.

In order to reduce the contact resistivity to below $1x10^{-8}\Omega cm^2$, the contact characteristics should be extensively investigated. Recently, we have measured the Schottky barrier height (SBH) of single crystal CVD-Al/Si contact [15]. Figure 5 shows the typical I-V curves of Al/(100)Si contact. The Schottky barrier height (ϕ) was determined using the $I_0=A^*T^2\exp(-\phi/kT)$, where I_0 is the saturation current density at V=0 and A* is the effective Richardson constant. The average Schottky barrier height of various contact size of 1.2-4 μm□ has been found to be ϕ_{CVD-Al}=0.66-0.69eV and $\phi_{sputter-Al}$=0.71-0.74eV, *i.e.*, ϕ_{CVD-Al} is lower than $\phi_{sputter-Al}$. There are two possibilities for the low SBH of CVD-Al. The first is the difference of the work function of *single crystal* and *polycrystal* Al. The second is the low surface state density of *single crystal* Al/Si interface. The origin of the low contact resistivity of CVD-Al/n^+-Si contact is considered to be its low SBH; Detail work is in progress.

We have found that CVD-Al/Si interface has a distinguishable feature as compared with the conventional polycrystal-Al/Si interface when the contact is annealed. Figure 6 shows the Si surface after removal of Al. The Si surface has not been eroded after the annealing of 450°C/N_2/30min. At the conventional pure-Al/Si interface, the alloy spike is known to be generated in Si, because Si is dissolved into Al with an atomic concentration of 0.5% at 450°C. On the other hand, the Si is not eroded at CVD-Al/Si interface after the annealing. The erosion-free characteristics is considered to be resulted from that CVD Al is *single crystal*.

The above results, low contact resistivity and erosion-free characteristics of CVD Al, show that CVD-Al/Si contact has a potential for Al/Si direct contact. However, the Schottky characteristics and contact resistance of *single crystal* CVD-Al/Si contact, and the alloy phase diagram of *single crystal* Al/single-Si interface should be investigated in more detail.

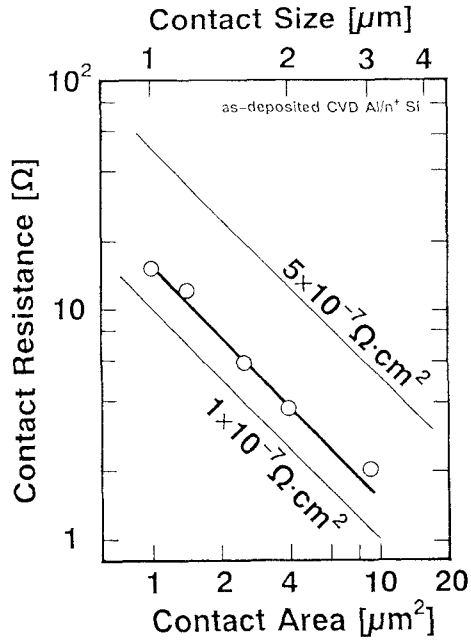

Fig. 4.
Contact resistivity as a function of contact size. The specific contact resistivity was found to be $2\times10^{-7}\Omega cm^2$.

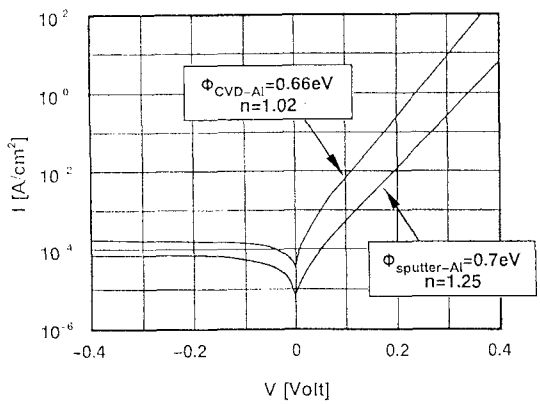

Fig. 5.
Typical I-V characteristics of Al/(100)Si Schottky contact.

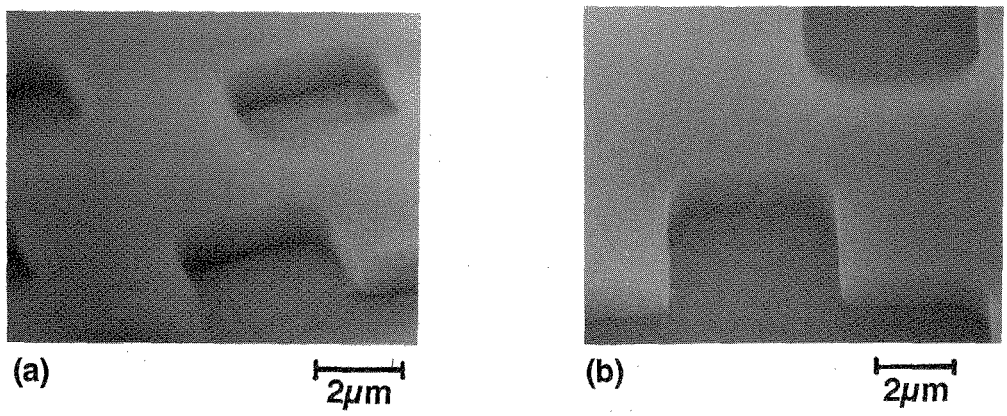

Fig. 6. SEM micrographs of the (111)Si surface after removal of Al. The annealing was carried out 450°C in N_2 ambient for 30min. (a) before annealing and (b) after annealing.

4. SAL²(Self-Aligned Selectively-Deposited-Aluminum) MOSFET

The selective Al CVD has another potential application for reducing the parasitic resistance of deep-submicron MOSFET. The parasitic resistance (sheet resistance of poly-Si gate electrode and source/drain regions, and contact resistance between the metal and the source/drain regions) should be reduced as low as possible in order to improve the delay time of deep-submicron MOSFET logic circuits. The SALICIDE (Self Aligned Silicidation) process where the Ti-silicide is formed on the poly-Si gate electrode as well as on the source/drain regions has been developed to reduce the parasitic resistance. However, the thickness of Ti-silicide is limited to be about 50nm in order to prevent the lateral growth of Ti-silicide on the side wall, so that the sheet resistance of poly Si-gate and source/drain regions are limited to be a few Ω/□.

We have recently proposed a new MOSFET structure named as SAL^2 (Self-Aligned Selectively-Deposited-Aluminum) MOSFET. In SAL^2 structure, the poly-Si gate electrode and the source/drain regions are covered with the selectively deposited Al. Figure 7 shows an example of a selective Al deposition onto n^+-poly-Si line and the Si surface [8]. One can see the Al is not deposited on the CVD-SiO_2 side wall. The resistivity of the CVD-Al/n^+-poly-Si line was dramatically reduced; the sheet resistivity of 0.3μm-thick n^+-poly-Si was 35Ω/□, and that

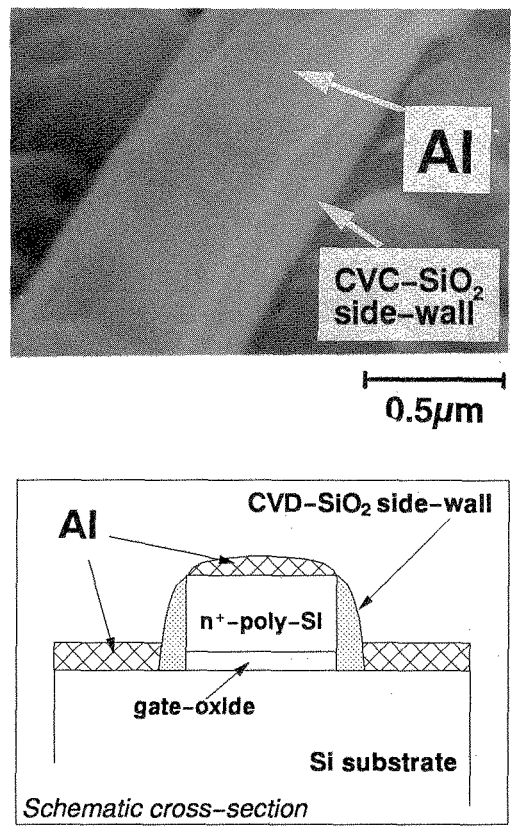

Fig. 7.
Selectively deposited Al onto the top of n+-Si line and the Si surface.

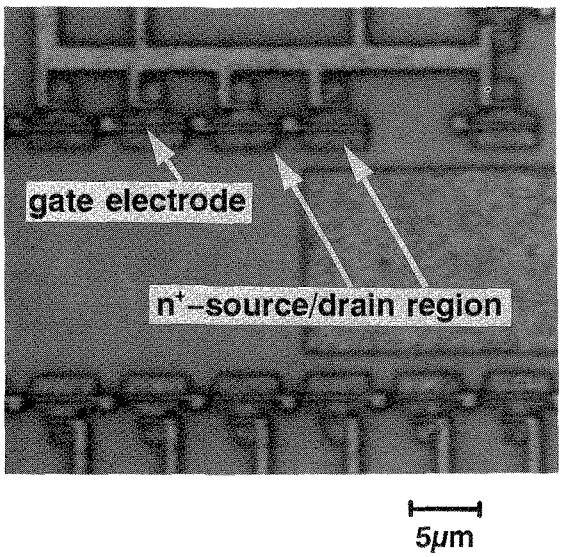

Fig. 8.
Nomarski photograph of SAL²-MOSFET circuit. The Al was selectively deposited on the n+-poly Si gate electrode and the n^+-source/drain region. The coding gate length are 0.2μm.

of 1μm-thick-CVD-Al/n^+-poly-Si was less than 30mΩ/□.

Figure 8 shows the E/E ring oscillator circuit of SAL² MOSFETs. The Al was selectively deposited on the gate electrode as well as on the source/drain regions. The coded gate length was 0.25μm and the design rule was 0.3μm.

5. SUMMARY

We have investigated area-selective chemical vapor deposition of Al using dimethylaluminum hydride and hydrogen. The features are (1) single crystal of Al on Si surface, (2) filling capability to deep-submicron via holes, (3) complete planarization of via holes by controlling the deposition mode, (4) low contact resistivity to n^+-Si, and (5) erosion free at Al/Si interface after annealing. The Al CVD technology has an excellent potential for application not only to the multilevel interconnects but also to the dramatic reduction of parasitic resistance of deep submicron MOSFETs.

ACKNOWLEDGEMENTS

This work was partially supported by the Grant-in-Aid for Priority-Area Research on "Photo-Excited Process" supported by the Ministry of Education, Science and Culture, Japan. Part of this work was carried out in the Superclean Room of the Laboratory for Microelectronics, Research Institute of Electrical Communication, Tohoku University.

REFERENCES

1. T. Amazawa and H. Nakamura, *Ext. Abs. of the 18th (1986 Int.) Conf. Solid State Devices and Materials*, Tokyo 1986, p. 755.
2. K. Masu, K. Tsubouchi, N. Shigeeda, T. Matano and N. Mikoshiba, Appl. Phys. Lett. **56** (1990) 1543.
3. T. Shinzawa, K. Sugai, S. Kishida and H. Okabayashi, *Workshop on Tungsten and Other CVD Metals for ULSI/VLSI Applications VI*, Tokyo 1989, p. 377.
4. K. Tsubouchi, K. Masu, N. Shigeeda, T. Matano, Y. Hiura, N. Mikoshiba, S. Matsumoto, T. Asaba, T. Marui, T. Kajikawa, *1990 Symp. on VLSI Technol.*, Honolulu 1990, p. 5.
5. K. Tsubouchi, K. Masu, N. Shigeeda, T. Matano, Y. Hiura, and N. Mikoshiba, Appl. Phys. Lett. **57** (1990) 1221.
6. K. Tsubouchi, K. Masu, K. Sasaki, and N. Mikoshiba, *1991 IEEE International Electron Devices Meeting*, Washington, DC 1991, p. 269.
7. K. Tsubouchi and K. Masu, J. Vac. Sci. Technol. **A10** (1992) 854.
8. K. Tsubouchi and K. Masu, Thin Solid Films **228** (1993) 312.
9. K. Tsubouchi, K. Masu and K. Sasaki, *Ext. Abs. of 1992 Int. Conf. on Solid State Devices and Materials*, Tsukuba 1992, p. 208.
10. K. Tsubouchi, K. Masu and K. Sasaki, Jpn. J. Appl. Phys. **32** (1993) 278.
11. G. S. Higashi, Y. J. Chabal, G. W. Trucks, and K. Pagahavachari, Appl. Phys. Lett. **56** (1990) 656.
12. K. Tsubouchi, K. Masu, M. Tanaka, Y. Hiura, T. Ohmi, N. Mikoshiba, S. Hayashi, T. Marui, A. Teramoto, T. Kajikawa, and H. Soejima, *Ext. Abs. of the 21st Conf. on Solid State Devices and Materials*, Tokyo 1989, p. 217.
13. K. Tsubouchi, K. Masu, M. Tanaka, Y. Hiura, T. Ohmi, N. Mikoshiba, S. Hayashi, T. Marui, A. Teramoto, T. Kajikawa, and H. Soejima, Jpn. J. Appl. Phys. **28** (1989) L2075.
14. K. Sasaki, K. Masu, K. Tsubouchi and N. Mikoshiba, *Ext. Abs. (The 52nd Autumn Meeting, 1991) of The Japan Soc. of Appl. Phys.*, Okayama, 1991, 11p-D-3. [in Japanese]
15. K. Masu, H. Matsuhashi, M. Yokoyama and K. Tsubouchi, to be presented at Advanced Metalization for ULSI Applications in 1993, Tokyo.