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Heterojunction diodes with fluorine-passivated SiC emitters formed by pyrolysis of di-*tert*-butylsilane

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A process has been developed to deposit stoichiometric polycrystalline SiC films at 775°C for potential uses as a wide band gap emitter material in silicon-based heterojunction bipolar transistors.

1. INTRODUCTION

Silicon carbide has recently attracted attention as a wide band gap emitter material for silicon heterojunction bipolar transistors [1,2]. SiC emitters have been shown to block hole back-injection in NPN transistors allowing heavily doped base regions to be used, while maintaining high current gain. This in turn permits a narrowing of the base region, improving high frequency performance. Although monocrystalline ß-SiC has been useful as wide band gap emitter in Si-HBTs, its epitaxial growth involves reaction of silanes and hydrocarbons at temperatures >1000°C. Such high temperatures are undesirable in processes for high speed bipolar transistors with a very thin (<50 nm), heavily doped base. To suppress dopant redistribution in the base during emitter formation, we have developed a process to deposit stoichiometric polycrystalline SiC film at 775°C [3]. In this paper we report the progress of our work including the additional capability of surface preclean and fluorine passivation. The material and electrical characteristics of the resulting heterojunction diodes are evaluated.

2. EXPERIMENTAL PROCEDURE

The CVD techniques that were used to deposit in situ phosphorus-doped SiC films have been described elsewhere [3]. The method involves pyrolysis of di-*tert*-butylsilane (DTBS) and tert-butylphosphine (TBP) vapor from liquid sources We performed in situ precleaning of the substrate surface in the base region with NF_3 to remove surface oxide and passivate potential traps or states prior to deposition of in situ phosphorus-doped SiC films at 775°C. Further incorporation of fluorine in SiC films was used to passivate dangling bonds in the amorphous material. The total thickness of approximately 40 nm SiC films was achieved in a stepwise deposition process which involves successively alternating between cycles of di-*tert*-butylsilane pyrolysis and NF_3 surface treatment.

The SiC films were capped with a further deposition of 300 nm polysilicon and rapid thermal annealed at 1075°C prior to emitter patterning.

The process and experimental matrix used to fabricate heterojunction diodes is shown below.

1. Starting material: P-type, 13-17 ohm-cm, Si(100).
2. Device well: standard device well formation using 700 nm thick field isolation.
3. Boron implant: boron was implanted into the device well silicon using the device well photoresist mask as an implant mask. Implant energy was 25 keV. Implant doses per sq.cm were as follows:
   - Group (a): no implant
   - Group (b): 1E13
   - Group (c): 1E14
   - Group (d): 1E15
   - Group (e): 1E16
4. SiC deposition: 40 nm thick layer of in situ doped N^+-SiC was deposited at 775°C.
5. Polysilicon deposition: 300 nm of in situ phosphorus-doped polysilicon was deposited
6. Polysilicon/SiC anneal: the composite film was rapid thermal annealed at 1075°C for 90 s.
7. Further processing in standard fashion including polysilicon patterning, BPSG deposition, contact formation, metal deposition and patterning, back-metal deposition and sintering.

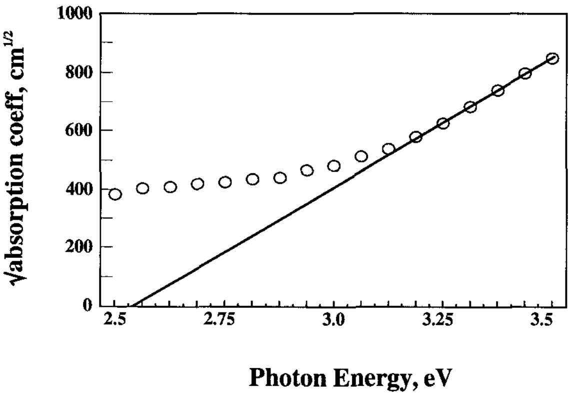

Figure 1. *Plot of square root of measured optical absorption coefficient versus photon energy for an 114 nm thick SiC film deposited on a quartz substrate which was rapid thermal annealed.*

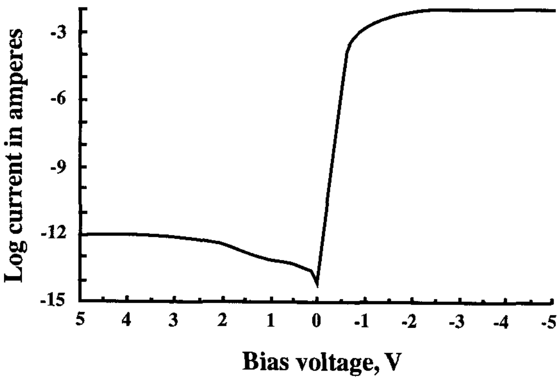

Figure 2. *Current-voltage characteristics of an N^+P heterojunction diode fabricated with N^+-SiC on P^+-Si(100) substrate of 15 Ω cm.*

The optical band gap of an in situ doped SiC film was evaluated from optical absorption measurements of a 114 nm thick film deposited on a quartz substrate which was annealed at 1075°C for 90 s. Any absorption by the quartz is accounted for by subtracting the baseline measurements of a blank quartz from the measured total absorption signals through the SiC/quartz. The results are shown in Figure 1 where the square root of the absorption coefficient is plotted against photon energy. By extrapolation to zero absorption the band gap for this SiC film is found to be 2.54 eV.

3. RESULTS AND DISCUSSION

To minimize leakage current associated with test equipment, the diodes thus formed were tested with bias potential applied to the substrate i.e. the prober chuck. The noise level measured on the prober, with the probe needle raised just above the devices, was about 4E-14 amps. The diodes were 0.01 cm X 0.01 cm in area and were completely isolated by 700 nm LOCOS field oxide. All diodes were discrete devices individually accessed.

Figure 2 shows a typical characteristic for an N^+P diode with substrate resistivity of 15 Ω cm. The turn on voltage for this diode is 0 V. For these devices reverse junction leakage at +5V reverse bias is in the range of 0.1 to 10 nA/cm^2. This reverse leakage does not increase with increasing substrate doping as evidenced by N^+P^+ diodes in Figures 3, 4 & 5. The utilization of carbide passivation and substrate doping can be jointly utilized to alter the electrochemical potential (or work function) at this material interface. This interface engineering can result in a predetermined value for the voltage at which forward bias commences. Hence the forward voltage drop can be made variable in an analogous manner to the threshold voltage of an MOS transistor, as shown in Figures 3, 4 and 5. The extent to which the

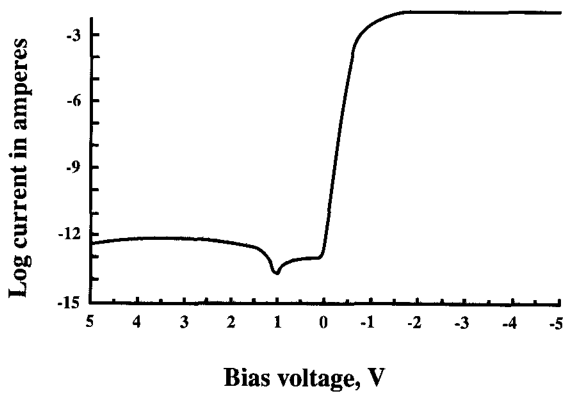

Figure 3. *Current-voltage characteristics of an N^+P^+ heterojunction diode fabricated with N^+-SiC on P^+-Si(100) substrate implanted with 1E14 boron ions/cm^2.*

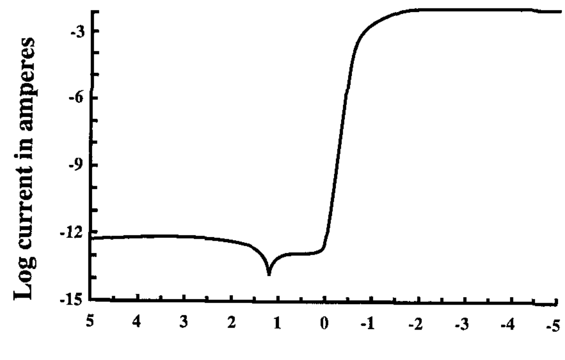

Figure 4. *Current-voltage characteristics of an N^+P^+ heterojunction diode fabricated with N^+-SiC on P^+-Si(100) substrate implanted with 1E15 boron ions/cm².*

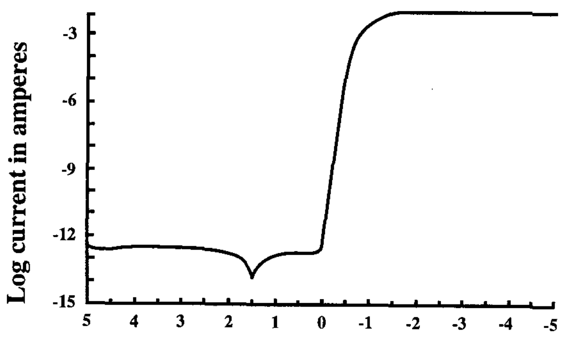

Figure 5. *Current-voltage characteristics of an N^+P^+ heterojunction diode fabricated with N^+-SiC on P^+-Si(100) substrate implanted with 1E16 boron ions/cm².*

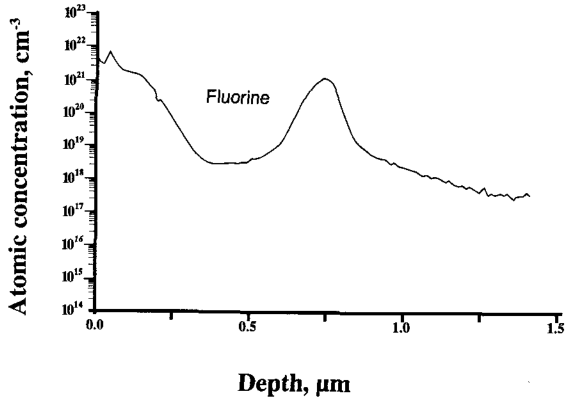

Figure 6. *A depth profile of fluorine in a heterojunction diode as measured by the SIMS technique.*

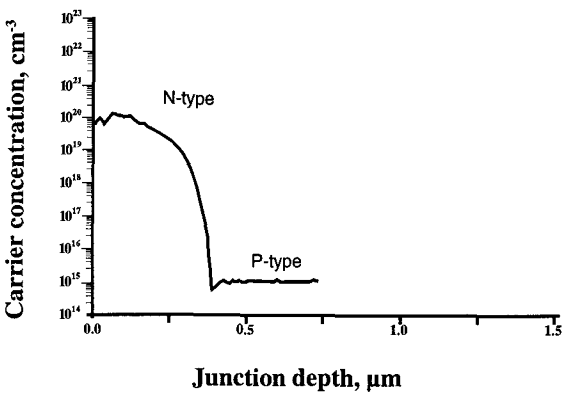

Figure 7. *Concentration profiles of N-type and P-type carriers in a heterojunction diode as measured by a spreading resistance probe, The P^+-Si(100) substrate was implanted with 1E15 boron ions/cm².*

surface can be engineered is presently under investigation as is the formulation of a device model. Assuming a standard diode equation, $I_d=I_s e^{qV/nkT}$, with the usual notation, the ideality factor "n" has been calculated to range from 0.93 (boron implant dose = 1.0E13 ions/cm²) to 1.11 (boron implant dose = 1.0E14 ions/cm²). The measured diode parameters are listed in Table 1.

Material analysis of some large area SiC emitters (100μm x 100μm) was performed. Auger analysis indicated near stoichiometric films as previously reported [3]. Figure 6 shows a depth profile of fluorine in a heterojunction diode as measured by the SIMS technique, while Figure 7 depicts concentration profiles of N-type and P-type carriers in the same heterojunction diodes as measured by a spreading resistance probe.

4. CONCLUSIONS

In conclusion, N^+P and N^+P^+ diodes have been fabricated with in situ phosphorus-doped, fluorine-passivated, stoichiometric, amorphous SiC film deposited on P-type Si(100) and capped with polysilicon. This technique results in interface work

Table 1.
Electrical characteristics of N^+P and N^+P^+ diodes fabricated with N^+-SiC emitter.

Boron implant dose (B^+/cm^2)	Saturation current I_S (A)	Turn-on voltage (V)	Ideality factor
nil	2E-15	0	0.95
1E13	8E-15	0	0.93
1E14	1E-13	0	1.11
1E15	2E-14	0	1.01
1E16	2E-14	0	1.00

function tailoring. Test results indicate that reverse leakage is between 0.1 and 10 nA/cm². Turn-on voltage is zero and the ideality factor approximately equals to 1.

5. ACKNOWLEDGEMENT

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