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AC HOT-CARRIER EFFECTS UNDER VERY FAST TRANSIENT STRESSING AND ITS IMPACT ON 16M DRAM

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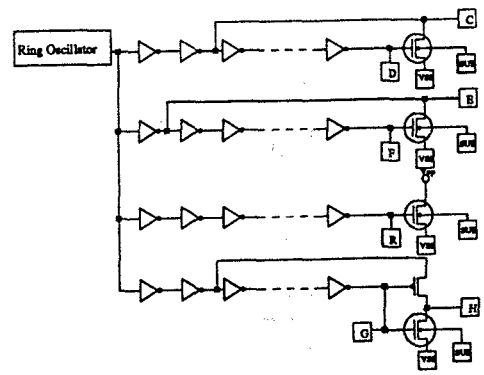
DC hot-carrier stress degradation in MOSFETs is well know but AC hot-carrier effects and its impact on the VLSI enviroment have not been thoroughly investigated. Recent observations have indicated that the dynamic form of stressing that occurs in a circuit operation with the drain and gate pulsing could cause more severe dgradation than the static form. But the rising rate dv/dt of the AC input signals supplied by the external signal generator is lowered by the wiring inductance. It suggests that past studies can't accurately estimate the degradation of MOSFETs in actual VLSI's. In this paper, on-chip hot-electron test/stress structures have been developed to investigate the dynamic effects in hot-carrier induced degradation of 0.5 micron n-MOSFETs under various pulsed operation conditions. The impact of hot-carriers on VLSI circuits are also studied extensively by stressing an actual 16M DRAM chip under active cycling.

1. INTRODUCTION

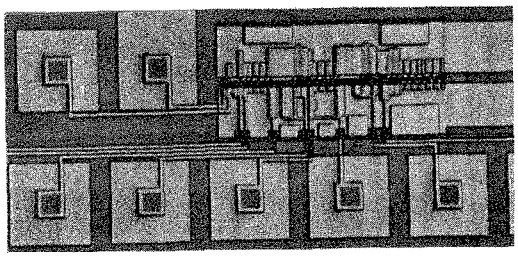
An understanding of the degradation phenomenom induced by hot-carriers in MOSFETs becomes more and more important in developing ULSIs using deep sub-micron technologies. There has been much interest in correlating the damage that results during static stress to damage under dynamic stress conditions. In particular, many of these studies have compared AC stress lifetimes to lifetimes predicted by quasi-static applications. In these reports, stress under AC or dynamic conditions was significantly worse than might be expected from quasi-static sum of DC stress [1],[2]. Much attention has been focused on this "enhanced AC stress" effect [3]. The operation frequency and switching time of the modern high-speed LSI's are around 100MHz and in the sub-nanosecond range, respectively. However, no work has been reported on degradation of MOSFETs suffering from various kinds of dynamic stressing with steep transient wave forms. This paper investigates the hot-carrier induced degradation of 0.5μm MOSFETs under different gate and drain voltage phases with sub-nanosecond transient times and the results are compared with not the quasi-static sum of static stressing data, but with the normal static stressing data. The impact of hot-carriers on VLSI circuits are also studied extensively by stressing an actual 16M DRAM chip using an 0.6μm CMOS process with its tox=150Å.

2. HOT-CARRIER DEGRADATION

The on-chip test structures have been fabricated with a 0.5μm CMOS process to evaluate hot-carrier induced degradation of MOSFETs under sub-nanosecond transient stressing conditions. The micro-photograph of the test pattern and the equivalent circuit configuration used for the AC stressing test is shown in Fig.1. Four kinds of gate and drain phases are used to find out the worst case gate and drain voltage phase conditions. Fig.3 shows measured wave forms for the drain and gate voltages at a supply voltage of 6V with an oscillation frequency of 135MHz.



a) Equivalent circuit diagram.



b) Micro-photograph of the test pattern.

Fig.1. Test pattern used for stress/test.

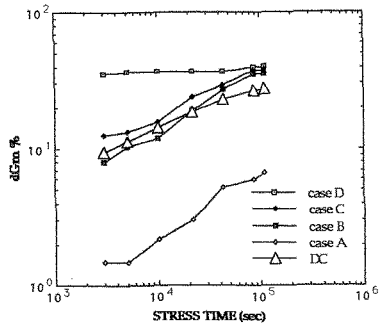
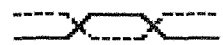
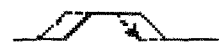
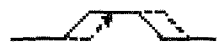
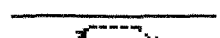


Fig.2. ΔGm as a function of stressing time at a supply voltage of 6V for AC vs. DC stressing.

Early reports showed that gate voltage transients (with constant drain voltage) lead to enhanced degradation, whereas drain voltage transients (with constant gate voltage), do not. [4],[5]. It was further claimed that the falling gate voltage edge, not the rising, is responsible for enhanced degradation. However, their conventional approach using an external pulse generator has produced controversial results [6] due to external parasitic effects associated with measurement setup. The test conditions for dynamic and static stressing as well as device structures are summarized in Table 1. The dependence of ΔGm as a fucntion of stressing time for four kinds of gate and drain voltage phases and DC stressing at a supply voltage of 6V is plotted in Fig.2. All of the gate/drain voltage phases, except for edge overlapping, shows more severe degradation than the DC stress. Of the four kinds of gate and drain voltage phases, case D shows the most severe degradation. Although the results for cases B and C are very similar, there is slightly more degradation in case C. As for case A, there is hardly any form of degradation compared with that of DC stressing degradation. The reason why case D shows the worst form of degradation is because of the combining of cases B and C, which when combined, accelarates the degradation process.

Table 1. Test structure and device structure.

Test Conditions	AC Stress @Vcc=6V f=135MHz tr,tf=0.5ns	Case A  Edge Overlapping Case B  Leading Vgs Case C  Leading Vds Case D  Static Vds with pulsed Vgs ——— = Vds ------- = Vgs
	DC Stress	Vcc=6.0V Vgs=2.5V
Device Structure	Drain Structure	LDD
	Size	0.5/10
	Tox	100Å

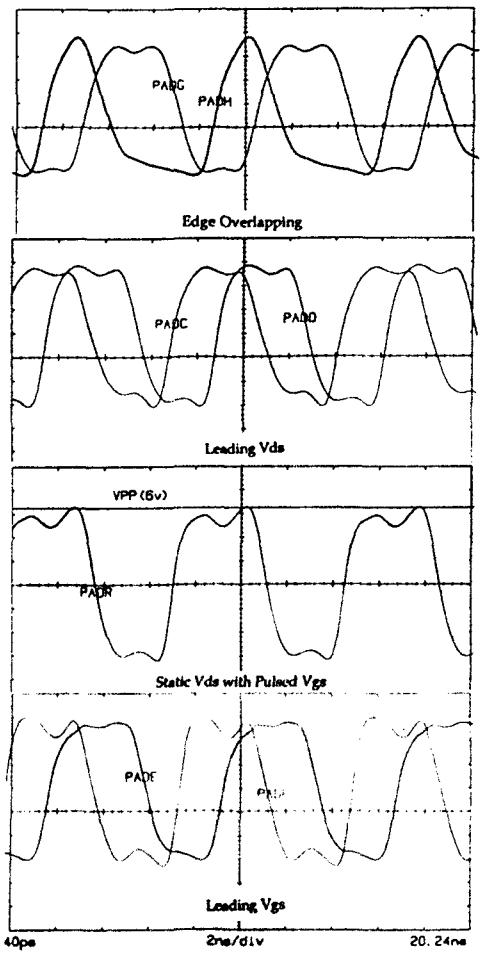


Fig.3. Measured wave forms

Previous studies have shown that case B is worse than case C, but our research indicates that the opposite is true. It suggests that past studies using external pulse generators can't accurately estimate the degradation of MOSFETs in actual LSIs. AC stressing followed by the increasing of off-state leakage currents are plotted in Fig.4. The enhancement of this leakage component could be due to the trapped charges near the drain region which causes a narrowing of the local depletion region. Since transistors in a circuit at a precharge cycle could be under a bias of zero volts on the gate and Vcc on the drain, the stand-by current will be increased due to the gate induced drain leakage current (GIDL) component. Fig.5 shows that hot-carrier effects on the stand-by and active currents. As shown in Fig.4, the stand-by current (Iec2) rapidly increases and peaks at a stressing time of 17 hours while after the peak, the stand-by currents gradually decreases. However, the active current is decreased as stressing time is increased. The reason behind this is because of the increasing of threshold voltage and the decreasing of the operating currents. The trac shmoo plot in Fig.6 shows the speed degradation under active cycling at Vdd=7V with a stressing time of 48 hours. It seems that the degradation of the complete transistor parameter has an impact on the the degradation of DRAM access time.

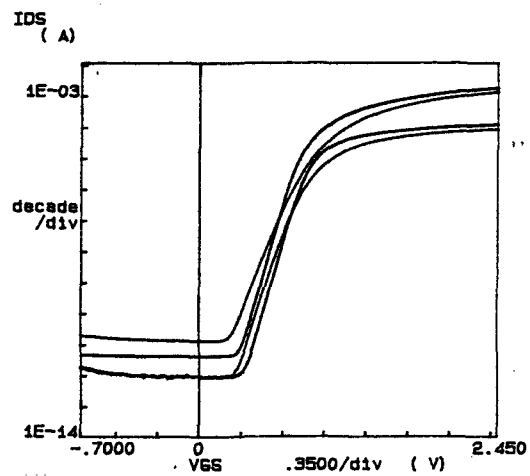


Fig.4. Saturation region sub-threshold curves for 0.5μm NMOS transistor before and after 12 hrs. of stress at 6V. Measured curves at Vds=0.5V and 3V.

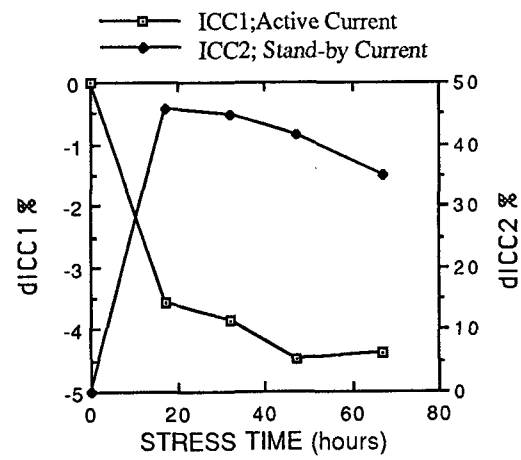
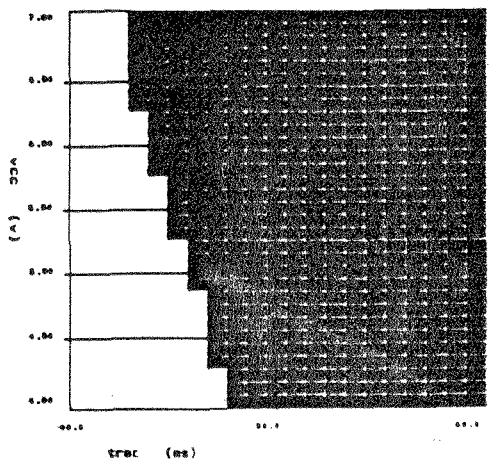
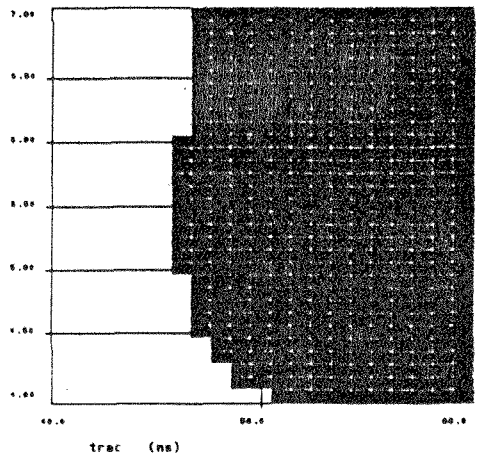


Fig.5. Active and stand-by current degradation vs. stress time.



a) Before stress.



b) After stress.

Fig.6. The shmoo plot for the DRAM chip stressed at 7V.

3. CONCLUSION

AC hot-carrier effects under very fast transient stressing are thoroughly investigated. The external parasitic free on-chip stress/test structures were used to find out the correlation between AC and DC stressing. Of the four kinds of gate and drain voltage phases, the pulsed condition of the static Vds with pulsed Vgs shows the most severe degradation. As the data shows, contrary to previous studies, there is more degradation in the case of leading Vds in comparison with the case of leading Vgs. In order to comprehend the effects of hot-carrier on DRAMs, a 0.6μm 16M DRAM chip has been stressed. The degradation of the observed stand-by currents characteristics has been attributed to the increase of off-state leakage current. It seems that the degradation of the complete transistor parameter has an impact on the degradation of the DRAM access time.

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