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Electronic Properties of Polycrystalline Silicon – Grain Boundary Segregation of Pd Atoms –

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Electronic properties associated with grain boundary segregation of palladium atoms in polycrystalline silicon have been investigated on the basis of measurements of electrical resistivity and Hall coefficient. It is found that the resistivity and its activation energy increase markedly with decreasing the annealing temperature, which is caused by palladium segregation at grain boundaries in Pd-doped polycrystalline silicon. Both of these results can be accounted for in terms of bond-length variation around Pd atoms as well as the case of Au-doped polycrystalline silicon in our previous work.

1 INTRODUCTION

Polycrystalline silicon (poly Si) has many important practical uses in modern electronic device technology. Unfortunately, degradation of device performance by impurity segregation at grain boundaries is a serious question in structures such as poly Si solar cells and thin film transistors. Extensive studies on this subject have been made for each of impurities P, As, B and Au in poly Si[1, 2, 3], but the general understanding of electronic properties associated with the impurity segregation at grain boundaries in poly Si is not complete.

The purpose of the present study is to extend to other impurity, Pd, in poly Si and to clarify the electronic properties associated with Pd segregation at the grain boundaries in poly Si on the basis of measurements of electrical resistivity ρ and Hall coefficient R_H.

2 EXPERIMENTAL PROCEDURE

Specimens of the present study originate from an n-type cast silicon with resistivity of $10^3\Omega$cm. The average grain size is about 300μm from the scanning-electron microscopy observation. The specimen were cut in a shape appropriate for Hall voltage and resistivity measurements.Then, they were mechanically polished and chemically etched in (HF/HNO_3) or ($HF/HNO_3/CH_3COOH$) mixture. Palladium thin layers were vacuum deposited on both sides (surfaces) of the specimen and conventional in-diffusion treatment was taken at temperature of 1150℃ for $15 \sim 30$ hours. Annealing treatments for palladium grain boundary segregation were then performed in a quartz tube furnace under argon flow for 20 hours (at maximum), which seems to be long enough to achieve possible Pd segregation at the grain boundary. Temperatures of the annealing were 740℃, 870℃, 900℃, 950℃ and 1000℃.

Measurements of electrical resistivity ρ using dc four-terminal method and of Hall coefficient R_H using dc method were performed at temperatures between 77K and 400K as a function of annealing temperature T_A. Conduction of the silicon sample, initially n-type, becomes p-type after addition of palladium, which shows that palladium is an acceptor impurity in polycrystalline silicon[4].

3 EXPERIMENTAL RESULTS AND DISCUSSIONS

Palladium is known to introduce an acceptor level ($E_{VB} + 0.34$eV) into the band gap of

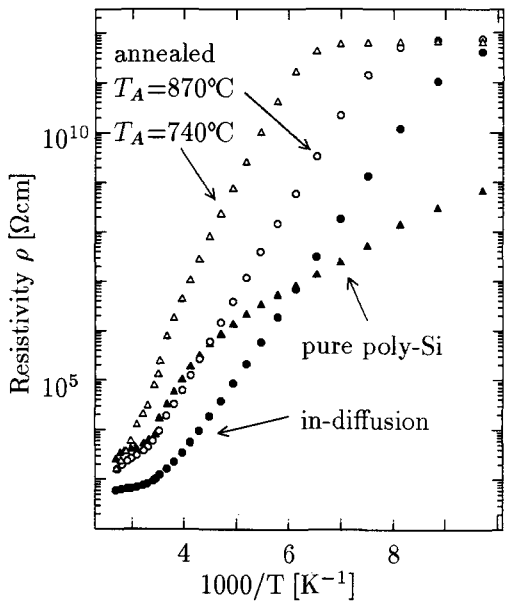

Figure 1: Experimental results of Arrhenius plots of resistivity ρ.

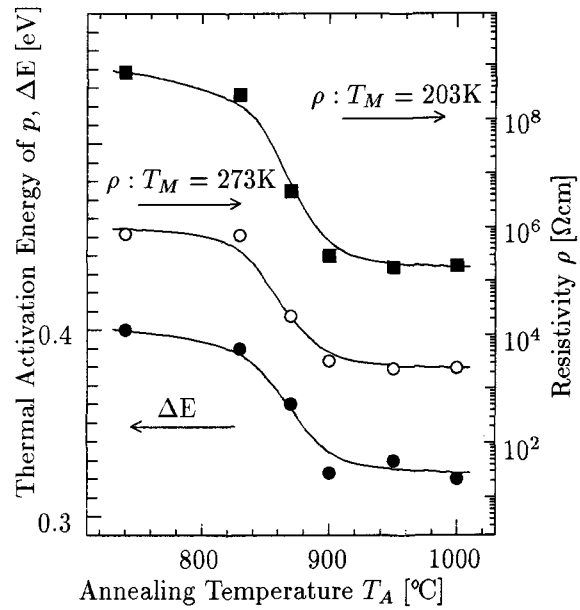

Figure 2: Thermal activation energy of p plotted against annealing temperature T_A.

silicon[4]. Therefore, it is of important to get information on the change in Pd deep level due to the introduction of lattice defects (grain boundaries and lattice dislocations), i.e., due to the variations of atomic configurations around the Pd atom.

In Fig. 1 are shown Arrhenius plots of resistivity ρ measured for the pure poly Si (not containing Pd), Pd in-diffused specimen and Pd-doped specimens annealed at temperatures of T_A = 740°C and 870°C. The details of annealing temperature, resistivity, hole concentration and thermal activation (ionization) energy of hole are summarized in Table 1. For p-type specimens, the activation energy (Pd deep acceptor) can be estimated by using the expression of temperature dependent hole concentration written as

$$p = N_V \exp(-(\mathrm{E_A} - \mathrm{E_{VB}})/kT), \qquad (1)$$

where N_V is the effective density of states of the valence band. $\mathrm{E_A}$ and $\mathrm{E_{VB}}$ represent the deep acceptor level and the top of the valence band, respectively. Using Eq.(1) and the experimental hole concentration p, we can determine the deep acceptor levels in poly Si doped with Pd as a function of the annealing temperature.

In Fig. 2, we present the activation energy ΔE, estimated from values of p estimated using those of ρ in Fig. 1, and resistivity ρ measured at 203K and 273K as a function of the annealing temperature T_A. From this figure, it is seen that values of ρ and ΔE increase monotonously as T_A decreases. This increase in ρ is thought to arise from reduction of holes caused by segregation of Pd. As shown in Fig.3, this reduction of holes is verified from the fact that hole concentration p decreases with decreasing the annealing temperature T_A. Here, the hole concentration p was estimated by the well known Hall-coefficient formula

$$R_H = V_H\, t/(BI) \propto 1/ep, \qquad (2)$$

where B, V_H, I and t are the strength of the magnetic field, Hall voltage, electric current and thickness of the specimens, respectively.

On the other hand, the increase in the activation energy presented in Fig. 2 can be explained as follows: It is pointed out in our previous work[3]

Specimen	Anneal. temp. T_A [℃]	Resistivity ρ [Ωcm]	Hole concentration p [cm^{-3}]	Activation energy of p ΔE [eV]
sipd-11	not-annealed	5.70×10^3	9.91×10^{13}	0.34
sipd-12	1000	2.41×10^3	4.10×10^{13}	0.32
sipd-13	950	2.37×10^3	2.90×10^{13}	0.33
sipd-14	900	3.32×10^3	1.77×10^{13}	0.32
sipd-15	870	1.88×10^4	5.50×10^{12}	0.36
sipd-16	830	7.05×10^5	(intrinsic)	0.39
sipd-17	740	7.54×10^5	(n-type)	0.40

Table 1: Temperature of annealing treatments and activation energy of resistivity for Pd-doped poly Si determined by experiments. Resistivities are measured at 0℃ and hole concentrations at room temperature.

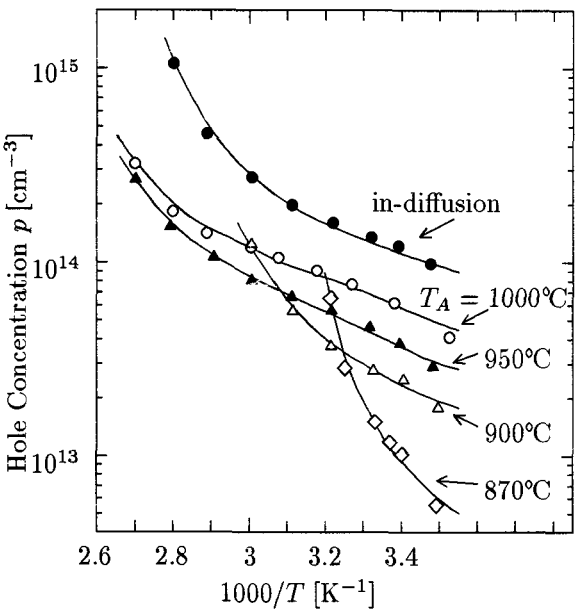

Figure 3: Arrhenius plots of hole concentration p for Pd doped (in-diffused) specimen and for Pd doped specimens annealed at 870, 900, 950, 1000℃ for 15 hours.

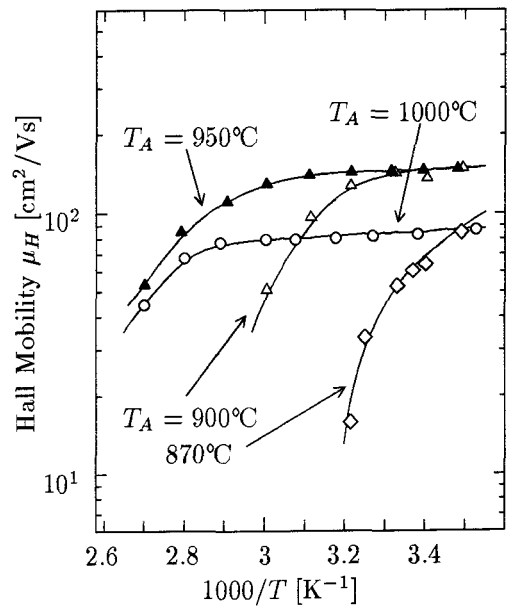

Figure 4: Arrhenius plots of Hall mobility μ_H for Pd doped specimens annealed at 870, 900, 950 and 1000 ℃ for 15 hours.

that the deep level associated with the transition metal impurities are very sensitive to atomic configurations of the lattice defects, especially to bond-length variations. Along this line, one can understand naturally that the segregated Pd impurities around the cores of the grain boundaries (or dislocations) can produce the deep energy levels quite different from those at perfect lattice sites. Therefore, we believe that as shown in Fig. 2 the increase in activation energy from ΔE = 0.32eV at T_A = 1000℃ to ΔE = 0.40eV at T_A = 740℃, where a value of 0.32eV is nearly

equal to that of Pd acceptor deep level in single crystal Si[4], should be caused by the segregated Pd impurities around the grain boundaries in poly Si. Such the segregated Pd nature is supported by the experimental results that as shown in Fig. 4, Hall mobility decreases markedly with decreasing the annealing temperature for the Pd-doped poly Si specimens presented in Table 1. This decrease in Hall mobility can be understood in terms of the hole trapping effect at the grain boundaries, which characterize the grain boundaries nature, in Pd-doped poly Si as well as the case of Au-doped poly Si presented in our work[2, 3].

Finally, we comment on the grain boundary segregation of Pd and the change in Pd deep level in poly Si. First, the Pd segregation at grain boundaries in poly Si can be explained as follows: It is known that the atomic configuration near the grain boundaries are distorted from that of the perfect lattice, and it becomes values of $2 \sim 3\%$ for the bond length change in poly Si[5]. Then, the distorted atomic sites are at high energy states, so that the grain boundary segregation of impurities is caused so as to reduce this high energy. In this respect, the electronic states of impurities segregated at the grain boundaries in poly Si are expected to be considerably altered compared with those in a perfect crystal Si. This is a physical origin of the deep level change associated with the segregated impurities at the grain boundaries in poly Si. Accordingly, the changes in Au deep level ($0.3 \sim 0.4$eV) observed for Au in poly Si were theoretically interpreted along this line [3]. For Pd in poly Si, the observed changes in Pd deep level can be understood on the basis of the Pd segregation at the grain boundaries (with changes in bond length) as well as the case of Au in poly Si, because Pd in Si shows almost a similar behavior as well as that in Au in Si.

These considerations are also supported as follows: It should be expected that the Pd atoms are easily segregated at the grain boundaries in poly Si, because of a large binding energy between Pd and the grain boundary, namely $\sim$ 0.3eV[5]. It must be noted that the direct observation of Pd segregation using SIMS was impossible for the Pd doped specimens containing Pd atoms of the order of $10^{16}\mathrm{cm}^{-3}$ estimated from diffusion data. Furthermore, we comment on the carrier trapping sites at the grain boundaries in poly Si affecting the reductions of resistivity, hole concentration and hole mobility shown in Figs.1, 3 and 4. The carrier trapping sites are estimated to be $\sim 10^{14}\mathrm{cm}^{-3}$[2] for poly Si with the observed average grain size of 300μm and using the trapping density of $3 \times 10^{12}\mathrm{cm}^{-2}$[6]. Value of $\sim 10^{14}\mathrm{cm}^{-3}$ is larger than that of $4 \times 10^{13}\mathrm{cm}^{-3}$ for the trapping sites at dislocations estimated from the dislocation density with $7 \times 10^{5}\mathrm{cm}^{-2}$ for poly Si used here. Thus, the hole trapping at the grain boundaries in poly Si should results in the dominant effect on the changes in resistivity, hole concentration and hole mobility observed here.

In conclusion, the present experimental results on Pd-doped polycrystalline silicon seem to contribute to the general understanding of electronic properties associated with the impurity segregation at the grain boundaries in polycrystalline silicon.

References

[1] M. M. Mandurah, K. C. Sarawat, C. R. Helms, and T. I. Kamins, J. Appl. Phys. **51**,5755 (1980).

[2] Y. Fujita and K. Masuda-Jindo, J. Appl. Phys. **67**,2965 (1990).

[3] Y. Fujita and K. Masuda-Jindo, J. Appl. Phys. **69**,3950 (1991).

[4] A. G. Milnes, Deep Impurities in Semiconductors, Wiley-Interscience, New York (1973)

[5] K. Masuda-Jindo, Trans. Iron Steel Inst. Jpn. **28**,842 (1988).

[6] J. Y. W. Seto, J. Appl. Phys. **46**,5247 (1975).