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Electron beam nano lithography and its application for 40 nm-gate MOSFETs

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A nanometer electron beam lithography system, which uses a Zr/O/W thermal field emitter (TFE) and has a 5-nm-diameter beam at an acceleration voltage of 100 kV, has been developed and used for fabricating sub-0.1μm gate MOSFETs. A 10-nm line in PMMA positive resist and also 10-nm line in Calixarene negative resist, both on a thick Si substrate were demonstrated by using the nano-electron beam lithography system. A chemically amplified negative resist was used as a single layer mask for MOS FET gate fabrication. After an improvement on resist process, the resist showed high resolution less than 40 nm width. Proximity effect correction was applied to the gate lithography, resulting in excellent line width control even less than 100 nm. Operation of a 40-nm-poly-silicon gate NMOSFET was confirmed.

1. Introduction

Reducing the device size leads the improvement of device performance such as switching speed and low power consumption and the integration of LSI's. The feature size of devices is becoming close to 0.1 μm. The lithography used in manufacturing process are optical technology using a mercury lamp g-line (λ=436 nm) and i-line(365nm). KrF excimer laser (248nm) as a light source is becoming used in 64 and 256 Mbit DRAM production with a feature size of 0.25-0.2μm. ArF excimer laser source and X-ray lithography are under intensive investigation for the production of 1Gbit and higher with a feature size of 0.18-0.1μm. Electron beam lithography has been used for the mask making (reticle) for optical lithography and for the development of device processes by means of direct writing. Recently, high-throughput electron beam lithography is intensively investigated by means of cell-projection exposure system, multiple beam system and so on. For the pattern size less than 100 nm (0.1μm), electron beam (EB) lithography with a use of Gaussian or point electron beam is only a way to delineate a pattern down to 10 nm. Therefore, nanofabrication technology has been extensively investigated using Gaussian electron beams[1-4]. This technology is used for the research of nanodevices. On the other hand, It is interesting that the limit size of small gate length MOSFETs [5-8]. The gate length is less than 0.1μm for 16Gbit DRAM. High density integrated circuits, and high switching speeds will be realized by using small gate MOSFETs. To fabricate MOS devices, it is necessary to make a poly-silicon gate by dry etching technology with good line width control. This paper describes the 50 kV nano-electron beam lithography system, its performance and its application of sub-0.1μm small gate MOSFET fabrication.

2. MOS device process using electron beam lithography

We used a nanometer electron beam lithography system[9] which uses Zr/O/W thermal field emitter (TFE) at an acceleration voltage of 50 kV. The system allows a small beam spot size of 5 nm at a current of 100 pA. A position of a wafer stage is measured by a laser interferometer with a resolution of 5 nm.

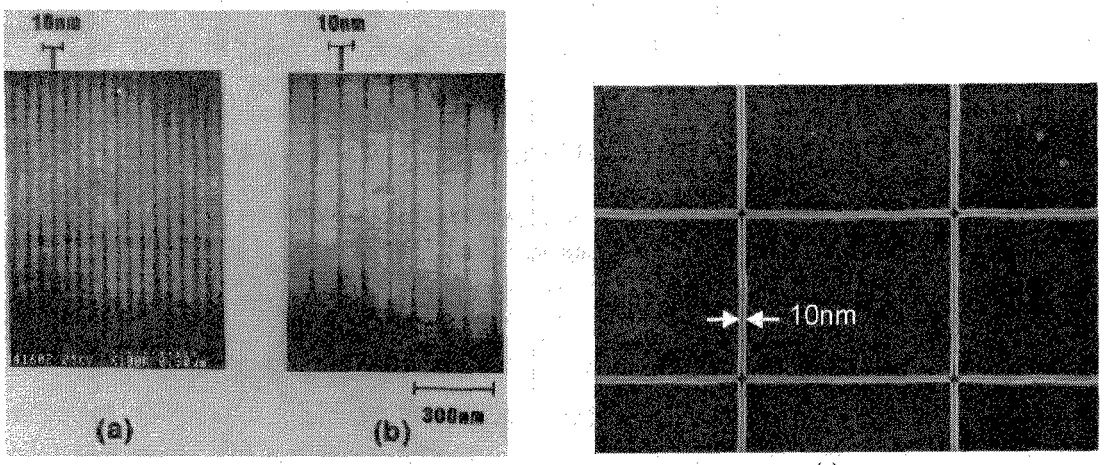

Figure 1 PMMA organic positive resist line pattern and Calixarene organic negative resist line pattern exposed by 50 kV Gaussian electron beam.

PMMA resist exposure was carried out to evaluate fine pattern exposure characteristics of the electron beam exposure system. PMMA is known to be a positive resist with the highest resolution. 30-nanometer-thick PMMA was spin-coated on a Si wafer and was exposed by 50kV electron beam. The line dose was 0.8 nC/cm. The PMMA was developed in a mixture of MIBK:IPA=1:3 for 1 minute and was rinsed in IPA for 1 minute. The point electron beam was line-scanned with spatial periods of 50 nm (Fig. 1(a)) and 100 nm (Fig. 1(b)). 10-nm line width patterns in the PMMA resist were obtained for both (a) and (b). The high acceleration voltage is expected to reduce the proximity effect and show high resolution lithography with small line periods. The high voltage is also expected to reduce the charge-up effect because of deep penetration. In figure 1 (c), fine negative resist patterns are also shown. This resist is called as Calixarene, which is a cyclic oligomers. The compounds is composed of a cyclic benzene nucleus, which has a diameter of about 1 nm. This chemical structure shows high resolution as shown in the figure. 10-nm line width line pattern was delineated on silicon wafer.

3. MOSFET fabrication process

3-1 Device fabrication process

Figure 2 shows a device process for sub 0.1μm gate MOSFET transistors.[11] The devices were designed similarly to those in Ref. 8 except that a single poly-silicon layer was used for the gate electrode. A 3.5nm-thick gate oxide was used to obtain high current drivability when a gate length is smaller than 0.1μm. The poly-silicon thickness was 150nm. We used a single layer chemically amplified resist as a mask to simplify the fabrication. An SAL601 (Shipley Ltd.) resist[12] with a thickness of 200-nm was coated on a 6" Si wafer. The resist thickness was determined based on an etching selectivity of 5 for the poly-silicon over the resist, to obtain high-aspect ratio poly-silicon gate patterns.

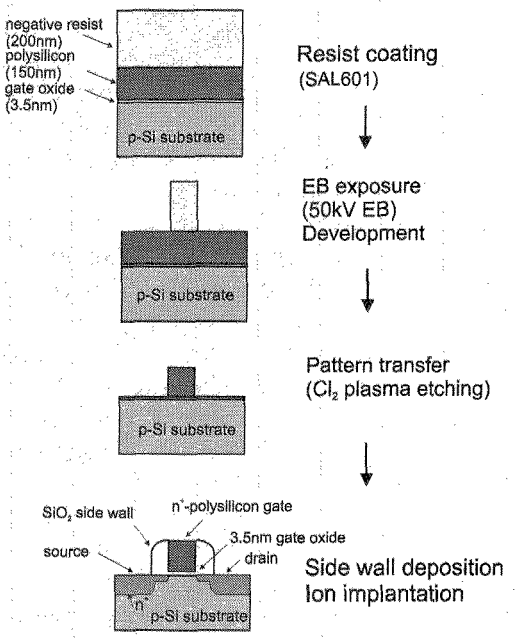

Figure 2 Si MOS device fabrication process by electron beam direct writing and dry etching for fabrication short gate

After exposing the resist by 50kV EB and developing the resist, the gate pattern was transferred into poly-silicon by time-modulated (TM) plasma etching[13] using Cl_2+SF_6+O_2 etching gas. The etching rate of the poly-silicon was 130nm/min with a uniformity variation of less than ±5%. The etching selectivity of the poly-silicon to SiO_2 was over 40. This etching method induces low charge-up, resulting in only a small amount of damage to the thin SiO_2 layer. Other lithography processes were performed using optical steppers.

3-2 Resist and dry etching process for Gate fabrication

The resist was spin-coated and pre-baked (PB) at 120 ℃ for 2 min. After EB exposure, the wafer was post-exposure-baked (PEB) at 100℃ for 2 min. Acid is produced by EB irradiation, and works as a catalyst to promote a cross linking chemical reaction of novolak resin during PEB process. Acid was re-produced during cross linking reaction, and perform chain reaction which leads high sensitivity for EB exposure. The acid was diffused then deteriorate a resolution. In our process, such high PB and low PEB are suitable for higher resolution,[14,15] because this process decrease the diffusion length of the acid.

After PEB, the resist was developed for 1 min in a TMAH(0.38N) developer. A high-normality developer was also suitable to achieve high resolution. The exposure characteristic of the SAL601 resist exposed for large area by 50 kV EB on a poly-silicon/SiO_2/Si wafer is shown in Fig. 6. The standard sensitivity was 50 μC/cm^2, which is about half that of conventional resist processes. Residual resist thickness was about 95%. On the other hand, the contrast ($\gamma=|\log(D^o/D_m)|^{-1}$) was over 4, thereby ensuring fine patterns with a high-aspect ratio

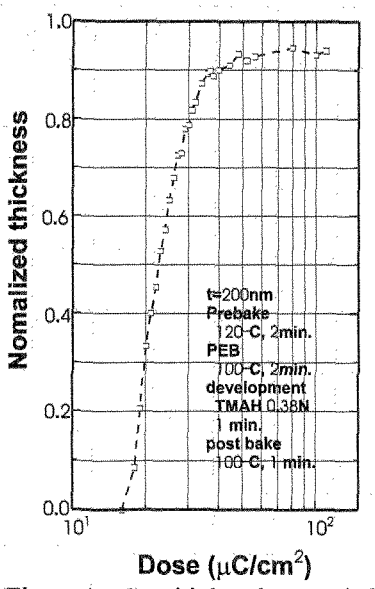

Figure 3 Sensitivity characteristics of SAL601 chemically amplified negative resist

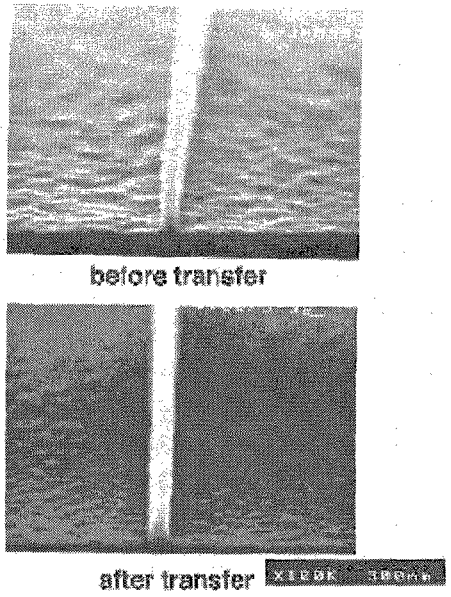

Figure 4 Fine resist pattern before pattern transfer and poly-silicon gate pattern after dry etching (before resist removal).

Figure 4 shows the fine 40-nm resist pattern on poly-silicon/SiO_2/Si. A minimum line width of 30 nm was obtained with a height of about 200 nm, and an aspect ratio over 6. A 30-nm line was exposed at 1200 μC/cm^2 by a single line scan, however, this resist pattern had low etching durability. Then we employed patterns with a size of over 40 nm for MOSFET fabrication. The poly-silicon gate pattern is shown in Fig. 4 (lower) after pattern transfer. The resist remained at a thickness of 70 nm, and there were no pattern width changes after the transfer. A thin gate oxide layer also remained on the wafer.

To obtain resist patterns with required width, electron dose for each pattern should be controlled due to proximity effect. For smaller patterns, higher exposure dose are required. Then we applied proximity effect correction for the gate lithography. We used Double Gaussian type energy intensity function for the correction. Patterns with accurate

sizes were obtained in a wide range from 40 nm to 10 μm.

3-4 Characteristics of minute NMOSFETs

We fabricated NMOSFETs with various gate lengths of more than 40nm on 6" wafers. Source-to-drain resistance at V_D=0.1V versus designed gate pattern width is plotted in Fig. 5. The good linearity indicated that the gate length was successfully controlled, even for gate lengths down to than 100 nm, by using proper proximity effect correction and a high energy nanometer electron beam. I_D-V_D characteristics are shown in Fig. 11 for the gate length of 70 to 40 nm. Well-behaved short channel characteristics were obtained down to a 60-nm gate length. Operation of a 40-nm gate FET was also confirmed, although weak punch-through occurred. Maximum transconductance (gm) at V_{DS}=1V was 580mS/mm for the 40 nm MOSFET.[7] It was confirmed that there is a possibility that the 40-nm gate MOS devices work practically by improving the other device parameters such as junction depth, substrate carrier density so on.

4. Summary

Nanometer electron beam lithography system with an acceleration voltage of 50 kV using thermal-field-emitter (TFE) gun has been developed. This system provides 5-nm-diameter electron beam at 50 kV and at a current of 100 pA. We demonstrated that 10-nm-width line patterns in PMMA resist on a thick Si substrate and 10-nm-width negative resist line in Calixarene..

The system was used to fabricate MOS devices with a small gate length on 6 inch Si wafer. A 40-nm-width SAL601 chemically amplified negative resist pattern with a height of 200 nm with an improved resist process. Fine single layer resist pattern was successfully transferred into poly-silicon layer by using Time-Modulated plasma etching.

We demonstrated that fine gate nMOSFETs with a gate length down to 40 nm can be fabricated by direct EB lithography and plasma etching. Finally, we confirmed that the operation and feasibility of a 40-nm gate nMOSFETs.

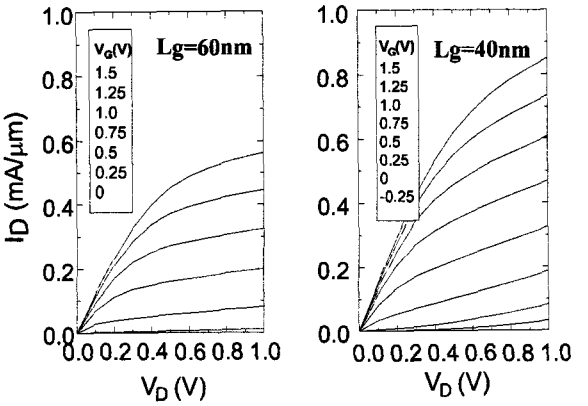

Figure 5 I_D-V_D characteristics of NMOSFETs with gate lengths of 70 to 40 nm using direct EB exposure and a single layer resist

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