Transactions of the Materials Research Society of Japan. Vol. 20


# Preparation and electrical characteristics of $SrTiO_3/IrO_2/Ir/TiN/Ti$ structure

**Masaaki NAKABAYASHI , Hiroshi ASHIDA ,Takafumi KIMURA , and Seigen OHTANI**
**Process development Division Fujitsu Limited**
**1-1 Kamiodanaka 4-chome Nakahara Kawasaki 211-88 Japan**

**Preparation and electrical characteristics were investigated for $SrTiO_3$(25-100nm) films on $IrO_2$(100nm) / Ir(50nm) / TiN(50nm) / Ti(30nm) electrodes. The capacitor cell of 4M-bit DRAM, 3.0 μm X 1.4 μm, were prepared to estimate electrical characteristics. At the result, good electrical properties were obtained, leak current density of $1X10^{-7}$ $A/cm^2$ (1.5V), and dielectric contents of 2 10. The $IrO_2$/ Ir / TiN / Ti films was effective to be use as bottom electrodes for thin film capacitors.**

## 1. INTRODUCTION

Recently, the films with high dielectric constant have applied for practical use in capacitor for 1G-bit DRAM. In capacitor fabrication, the most troublesome problem is the choice of an appropriate electrode material, because the capacitor of DRAM must connected directly on Si plug to use effective cell area. Formation of oxide caused bad contacts when oxide dielectric films are deposited directly on Si plug. Therefore a barrier layer between the dielectric layer and Si plug is required. Pt / Ta is well known electrode for oxide high dielectric materials.[1][2][3][4] Pt lattice matches well high $SrTiO_3$ and Pt is less reactive with $SrTiO_3$. However, An insulating $TaO_x$ layer formed after deposition of $SrTiO_3$ film. Oxygen diffusion were easily taken by sputtering process in oxygen atmosphere at temperature higher than 600°C and Ta was oxidized. An Ability of Pt / Ta as a barrier layer to oxygen diffusion is very poor. Properties of Ir is similar to those of Pt. Ir is oxidized by high temperature annealing in oxygen atmosphere. In this study, we evaluated $IrO_2$/ Ir / TiN / Ti electrode for oxide dielectric materials.

## 2. EXPERIMENTAL PROCEDURES

TiN / Ti was used for barrier layer to protect Si diffusion. These films were prepared by conventional sputtering method. Deposition condition was showed in a table 1. TiN(50nm) / Ti(30nm) were deposited on cleaned Si wafer at 350°C. And $IrO_2$(100nm) / Ir(50nm) were grown on TiN / Ti coated Si wafers. $IrO_2$/ Ir was used for barrier layer to protect $O_2$ diffusion. $SrTiO_3$ films were reactivily sputtered on $IrO_2$/ Ir / TiN / Ti / Si substrates at 450°C. The thickness of $SrTiO_3$ films were ranging

from 25 to 100nm. Kelvin patterns and capacitor cell of 4M-bit DRAM were prepared to mesure electrical characteristics; contact resistance, capacitance, and leakage current density. The crystallinlty of the film was measured using XRD. Surface morphology was examined by SEM. Electrical measurement was done two types of contacts ; between the top electrode upper $SrTiO_3$ to the $IrO_2$ directly or the backside of Si wafer. The capacitance and leakage current were valued with LCR mater , picoammeter , DC voltage. Dielectric constants of the capacitor cell were calculated from capacitance measurement at 100kHz.

## 3. RESULT AND DISCUSSION

### 3.1 Properties of $SrTiO_3$ / $IrO_2$ / Ir / Si

XRD pattern of $SrTiO_3$ / $IrO_2$ / Ir / Si structure was shown in figure 1. Poly crystalline $IrO_2$, Ir, and $SrTiO_3$ were deposited on Si wafer. Electrical measurement were measured between the top electrode of $SrTiO_3$ to $IrO_2$ directly. Leak current density versus voltage characteristics were shown in figure 2, Film thickness of $SrTiO_3$ were 25nm (x) and 50nm (□) , respectively. The dielectric constant properties were 200 (25nm) and 250 (50nm) , respectively. The leakage current were both $1 \times 10^{-7}$ A/cm$^2$ at 2V. $SrTiO_3$ could be as thin as 25nm on $IrO_2$ / Ir for bottom electrode. An ability of $IrO_2$ / Ir as a barrier layer is very effective to prevent reaction with $SrTiO_3$.

### 3.2 Contact resistance

Contact resistance between $IrO_2$ / Ir / TiN / Ti and ion inplanted Si wafer were estimated useing Kelvin patterns with contact hole of $\phi$ 0.72μm. Leakage current versus applied voltage characteristics was shown in figure 3. Current was proportion to voltage. This proportional relation inhibited to get ohmic contact between $IrO_2$ / Ir / TiN / Ti and Si wafer. Contact resistance was 19 Ω. (contact hole of $\phi$ 0.72μm) To test suitability for high temperature processes, these patterns were annealed in oxygen atmosphere of 760 Torr for 30 min. Annealing temperature was ranging from 450°C to 600°C. Figure 4 was shown in the contact resistance versus annealing temperature. Circles and squares in figure 3 mean top electrode positive and negative at 2V, respectively. The same value between ○ and □ were kept until annealing temperature of 450°C. This indicates that $IrO_2$ / Ir was sufficient to prevent oxygen diffusion up to 450°C temperature.

### 3.3 Preparation of 4M-bit capacitor cell

4M-bit capacitor or cell were prepared to estimate electric properties, capacitance and leakade current density. The area of capacitor cell was 3.0μm x 1.4μm x 500. This area correspond to that of 4M-bit DRAM cell. Film thickness of $SrTiO_3$ were 100nm.

Figure 5 shows SEM image. The leakage current density versus applied voltage was shown in figure 6. The leakage current was 1 x 10$^{-7}$ A/cm$^2$(1.5V). The dielectric constant was 210. These value independent of measuring from $IrO_2$ surface or backside of Si wafer. This indicates that no uniform insulating phases were formed between $IrO_2$ / Ir / TiN / Ti and Si wafer.

## 4. CONCLUSION

Preparation and electrical characteristics were investigated for prepared $SrTiO_3$ films on $IrO_2$/ Ir/ TiN / Ti. Capacitor cells of 4M-bit DRAM and Kelvin patterns were prepared to estimate electric properties. Contact resistance was 17 Ω with ϕ 0.72μm of contact hole. Leakage current and dielectric constant were 200 and 1x10$^{-7}$ A/cm$^2$(1.5V), respectively. The $IrO_2$/ Ir/ TiN / Ti were effective to be use as bottom electrodes for thin film capacitors.

## REFERENCES


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Table 1. The typical suputtering conditions of $SrTiO_3$, $IrO_2$, and Ir films.

| Film | Power | Flow rate | Pressure | Temp. |
|---|---|---|---|---|
| $SrTiO_3$ | 500W | Ar 40sccm<br>$O_2$ 5sccm | 10mTorr | 450-500° C |
| $IrO_2$ | 300W | Ar 40sccm<br>$O_2$ 30sccm | 10mTorr | RT. |
| Ir | 500W | Ar 40sccm | 5mTorr | 500° C |

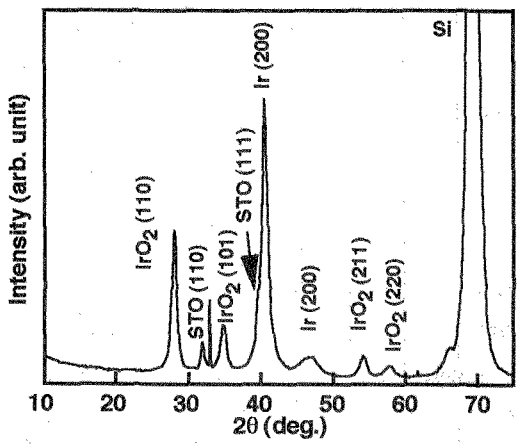


Figure 1. The X-ray diffraction pattern.

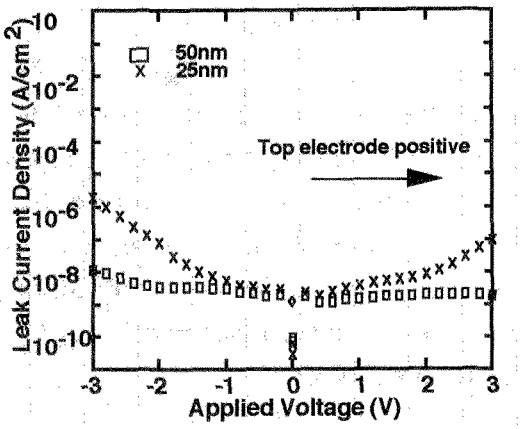


Figure 2. Applied voltage dependence of the leak current density

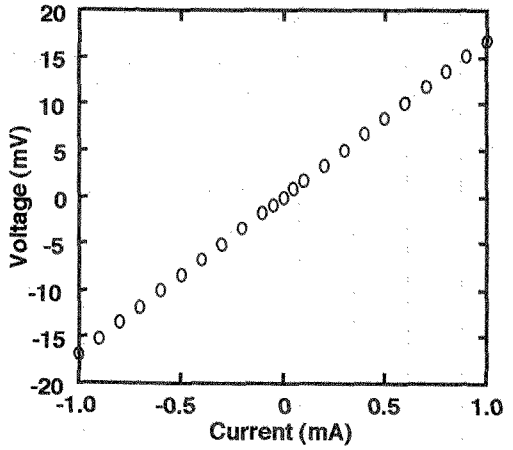


Figure 3. Current - voltage characteristics

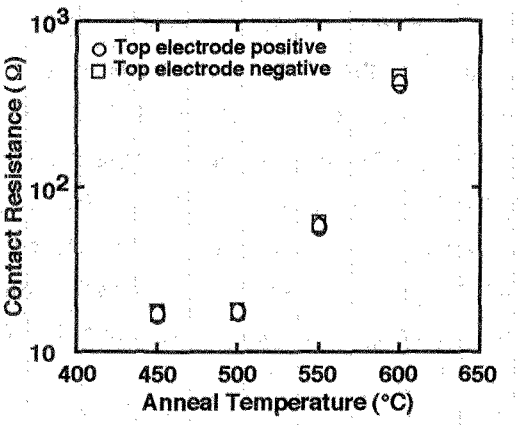


Figure 4. Annealing temperature dependence of the dielectric constant value.

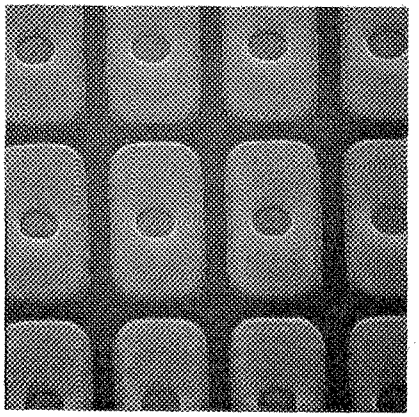

Figure 5. SEM imarge of capacitor cell of 4M-bit DRAM,3.0μmx1.4μm.

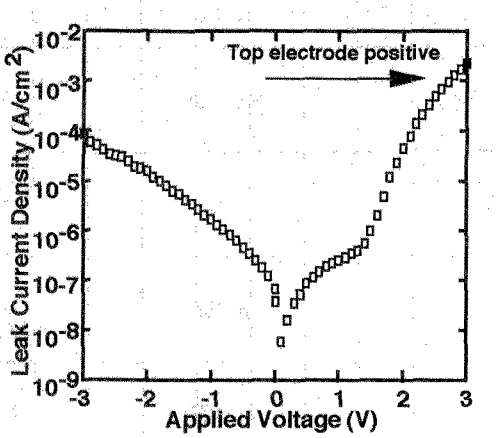


Figure 6. Applied voltage dependence of the leak current density of 3.0 μmx1.4μmx500