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CHARACTERIZATION OF $SrBi_2Ta_2O_9$ FILMS PREPARED ON Si SUBSTRATES BY SOL-GEL METHOD

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$SrBi_2Ta_2O_9$ films are prepared by the sol-gel technique on n-Si(100) substrates. Ploy-crystalline $SrBi_2Ta_2O_9$ films can be obtained on Si substrates and the crystallite orientations of the film on Si were similar to those of the films prepared on $Pt/Ti/SiO_2/Si$ substrates. It is shown by the secondary ion mass spectrometry (SIMS) that the inter-diffusion was suppressed even at such high annealing temperatures, which is in contrast to the PZT films which strongly diffuses into Si substrates. The C-V plot showed a hysteresis loop with a counterclockwise trace with a memory window of 0.3V for ±4V sweep due to the ferroelectric nature of the $SrBi_2Ta_2O_9$ films.

1. INTRODUCTION

Recently, there has been a growing interest on ferroelectric materials for non-volatile memory applications. Non-volatile memories using ferroelectric capacitors have been widely studied, recently, which utilize basically destructive read operations. On the other hand, nonvolatile memories using metal-ferroelectric-semiconductor field-effect transistors (MFSFETs) make non-destructive read operation possible. In addition, MFSFETs can be used as adaptive-learning analog memories in neural network systems [1]. However, preparation of the ferroelectric thin films directly on Si substrates with good interface is very difficult because of the chemical reaction of Si and ferroelectric materials. Particularly, it is well known that ferroelectric $PbZrTiO_3$(PZT) films easily react with Si and inter-diffusion of Pb and Si at the PZT/Si interface occurs even at temperatures as low as 500 °C [2,3]. Nakao *et al.* [4] reported MFMIS (metal-ferroelectric-metal-insulator-semiconductor) FET structure using PZT and SiO_2 as a ferroelectric film and a gate insulator. In this structure, the excellent interface properties of SiO_2/Si is available. However, it becomes difficult to apply sufficient voltage to the PZT film because the dielectric constant of PZT films is much higher than that of SiO_2 (ε_r=3.9). Consequently, it needs high operation voltage to apply large enough voltage to reverse the polarization of the PZT film.

Hence, the search of the other ferroelectric materials is an important issue to fabricate MFSFETs. The use of ferroelectric fluorides such as $BaMgF_4$ is one of the interesting approaches, however, MFSFETs using $BaMgF_4$ films still suffer from short retention time [5, 6]. On the other hand, $SrBi_2Ta_2O_9$ (SBTO) has attracted much attention because it has superior fatigue-free properties [7, 8] and many reports on the preparations and applications of ferroelectric SBTO films have been reported [9,10]. However, the electrical and interface properties of SBTO films formed on Si substrates is not clear at present. In this paper, we report the preparation and characterization of SBTO films grown on Si and SiO_2/Si substrates by the sol-gel method.

2. EXPERIMENTAL

SBTO films were prepared by the sol-gel method directly on n-Si(100) substrates. $Pt/Ti/SiO_2/Si$ substrates were used for the measurements of the P-E hysteresis of the grown SBTO films. SBTO sol-gel solution was spin-coated and consolidated at 500 °C for 10 min. After the above process was repeated several times, the films was annealed at 750°C for 30 min in an oxygen ambient. The thickness of the SBTO film was varied from 100 nm to 240

nm. Then after Pt top electrodes were formed by the vacuum evaporation technique, the samples were annealed again at 800 °C for 30 min in an oxygen ambient. Electrodes area is $3x10^{-4}$ cm^2 (200 μm in diameter).

X-ray diffraction (XRD) measurement was employed to characterize the crystalline quality of the SBTO films. Electrical characteristics of the SBTO films grown on Si substrates were characterized by the capacitance-voltage (C-V) measurements. Inter-diffusion of the SBTO films and Si substrates was measured by the secondary ion mass spectrometry (SIMS).

3. RESULTS AND DISCUSSION

3.1 Crystalline Quality

Fig.1 shows XRD patterns of SBTO films grown on (a) Pt/Ti/SiO_2/Si and (b) Si substrates, respectively. It is found that ploy-crystalline SBTO films were obtained on both Pt/Ti/SiO_2/Si and Si substrates. As shown in Fig. 1, diffraction peaks from (105), (110), (200) and (215) crystallites are observed for SBTO films formed directly on Si substrates, which are also observed for the films prepared on Pt/Ti/SiO_2/Si substrates. To clarify the ferroelectric characteristics of the SBTO films used in this work, P-E hysteresis loops were measured for the SBTO formed on Pt/Ti/SiO_2/Si substrates as shown in Fig. 2. Obtained remanent polarization (Pr), coercive field (Ec), and relative dielectric constant (ε_r) are 6.3 μC/cm^2, 46 kV/cm, and 250, respectively. These values are similar to those reported in the literature.

Next, interdiffusion of SBTO films were studied by measuring the depth profiles of constituent elements using secondary ion mass spectrometry (SIMS). It is found in Fig. 3 that the inter-diffusion is suppressed and rapid change of Sr, Bi, Ta, and Si are observed at the SBTO/Si interface. This is in contrast to the PZT films which strongly diffuses into Si substrates even at low temperatures around 500 °C. It is worth noting that the SBTO films used in this work were first annealed at 750 °C followed by the second annealing at 800 °C and that each annealing time was as long as 30 min. This asset makes the SBTO films very promising for MFSFET applications.

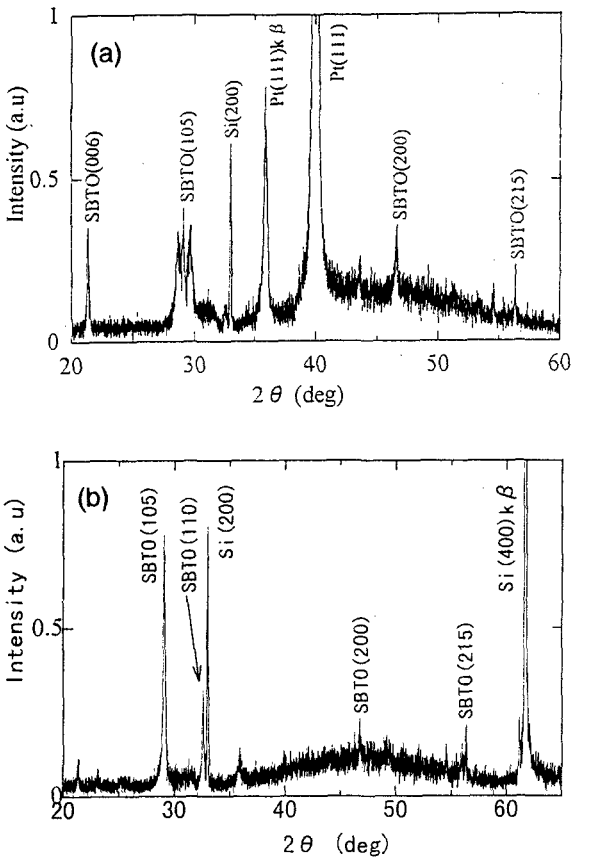

Figure 1 X-ray diffraction patterns of SBTO films grown on (a) Pt/Ti/SiO_2/Si and (b) Si substrates.

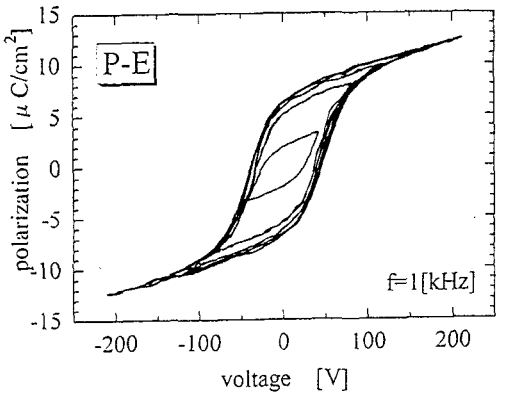

Figure 2 P-E hysteresis loops of SBTO formed on Pt/Ti/SiO_2/Si.

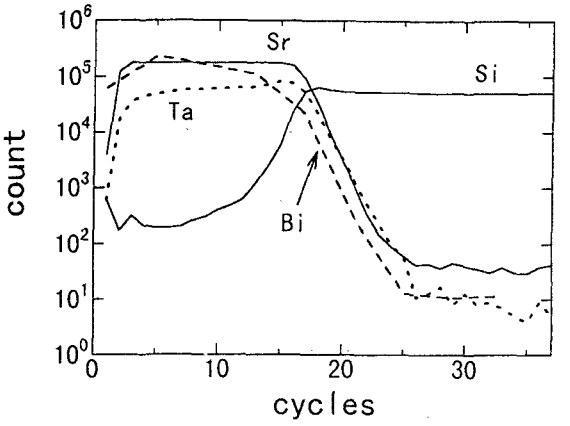

Figure 3 Depth profiles of constituent elements of the SBTO film prepared on Si substrate measured by SIMS.

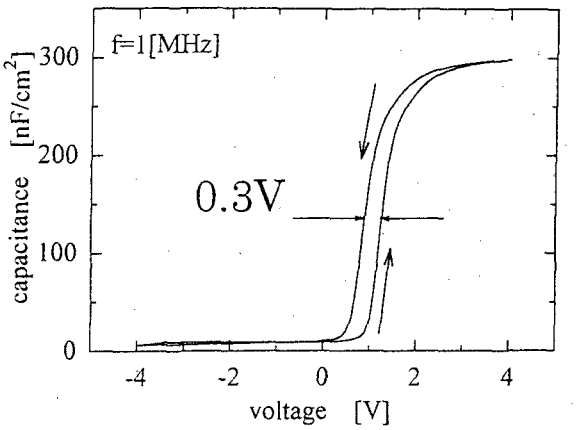

Figure 5 Capacitance-voltage (C-V) characteristics of SBTO/Si structure.

3.2 Electrical Properties of SBTO/Si Structure

Next, capacitance-voltage (C-V) and current voltage (I-V) characteristics were measured at room temperature. The SBTO film was directly grown on n-Si(100) substrate with a thickness of 180 nm. The I-V characteristics is shown in Fig. 4. Reasonably low leakage current was obtained below 4 V. However, when the applied voltage is larger than 4 V, the leakage current suddenly increases as shown in Fig. 4. Hence, for the C-V measurements, the applied voltage was varied from -4V to +4V. The

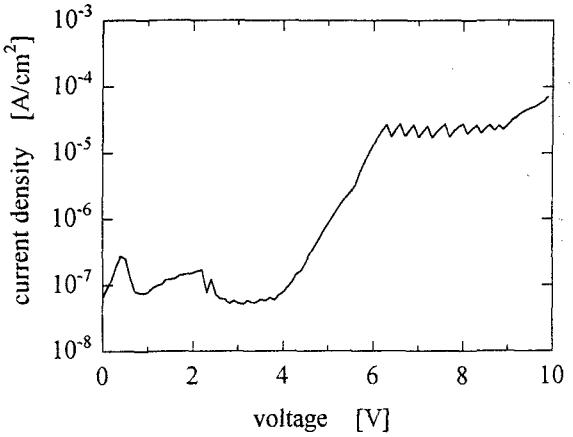

Figure 4 Current-voltage (I-V) characteristics of SBTO/Si structure.

C-V plot is shown in Fig. 5. A hysteresis loop with a counterclockwise trace was clearly observed. This is due to the ferroelectric nature of the SBTO film and a memory window is estimated about 0.3V. The memory window in the C-V plot corresponds to the twice of the coercive voltage. If it is assumed that the coercive field of SBTO films on Si substrates is 46 kV/cm as obtained for the SBTO film on Pt/Ti/SiO_2/Si substrates (Fig. 2), the memory window in this structure should be 1.6V (=2Vc). The small memory window of 0.3 V obtained here is because the low-dielectric constant layer, probably an SiO_2 layer, was formed at the SBTO/Si interface during the film growth process. Hence, the voltage applied to the SBTO layer becomes small. By measuring the capacitance with varying the SBTO film thickness, the thickness of the SiO_2 layer is estimated to be about 9 nm. Because of the presence of this SiO_2 layer, most of the voltage applies to the SiO_2 layer. The voltage actually applied to the SBTO layer is estimated to be only 1 V for a total applied voltage of 4 V. Hence, a coercive voltage obtained from a P-E hysteresis loop for ±1 V sweep should be used to estimate the magnitude of the memory window. In our experiments, the 2Vc value calculated from the P-E characteristics for ±1 V sweep is about 0.2 V, which is close to the observed memory window of 0.3 V.

3.3 Electrical Properties of SBTO/SiO_2/Si Structures

As shown in Fig. 4, a low breakdown voltage is one of the problems when SBTO films are directly deposited on Si substrates. Since the SiO_2 layer was automatically formed during the growth process, we intentionally formed the thin thermal oxide before the SBTO film growth. The thermal oxide can improve not only the interface properties but also I-V characteristics, which allow us to apply higher voltages. SiO_2 layers were formed by the conventional thermal oxidation process using O_2. The thickness of the SiO_2 layer was varied from 12 nm to 40 nm. Figure 6 shows the I-V characteristics of the SBTO/SiO_2/Si structure when the SiO_2 thickness is 40 nm. The thicknesses of the SBTO is 175 nm. It is found that the breakdown voltage is above 30 V. Hence, we measured the C-V characteristics with varying the applied voltage from -28 V to +28 V as shown in Fig. 7. Normal C-V curve was observed even though the applied voltage was as high as ±30 V. A counter-clockwise trace of C-V plot is clearly seen in Fig. 7. Since no hysteresis was observed when the applied voltage is small, the counter-clockwise hysteresis obtained here is caused by the ferroelectric SBTO film.

The memory window determined from Fig. 7 is 0.66 V, which is more than twice as large as that obtained for the directly deposited SBTO film on Si substrates. However, to obtain a memory window of 0.66 V, a large operation voltage is necessary in this structure. This is because the structure has a relatively thick (40 nm) SiO_2 layer and hence most of the voltage is focused on the SiO_2 layer. To decrease the operation voltage, we next reduced the SiO_2 thickness from 40 to 12 nm. Figure 8 shows I-V characteristics of the SBTO/SiO_2/Si structure for a SiO_2 thickness of 12 nm. The thicknesses of the SBTO is 175 nm. It is found that the breakdown

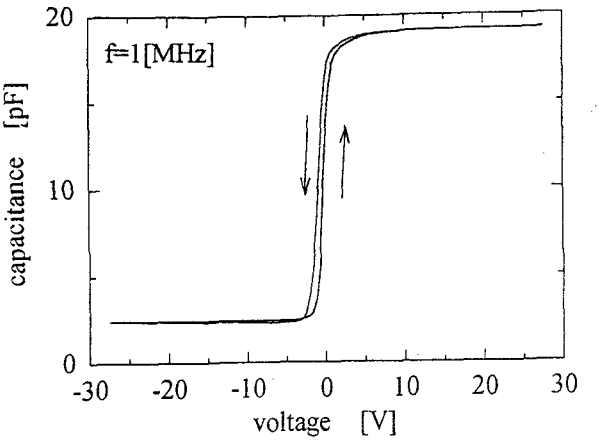

Figure 7 C-V characteristics of SBTO(175nm)/ SiO_2(40nm)/Si structure.

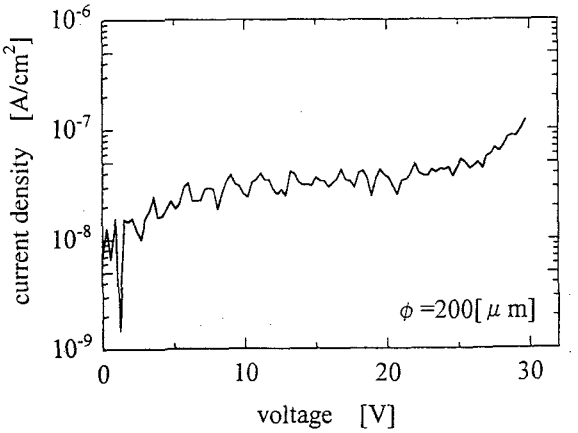

Figure 6 I-V characteristics of SBTO(175nm)/ SiO_2(40nm)/Si structure.

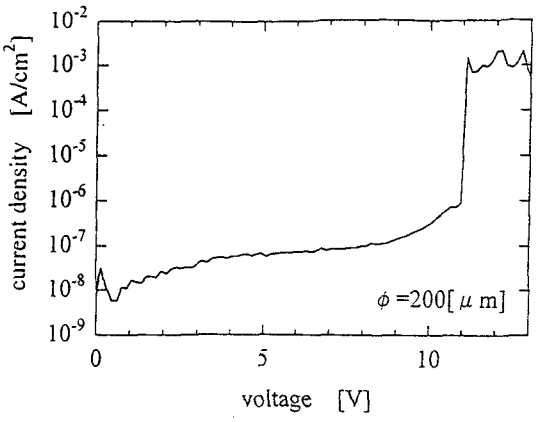

Figure 8 I-V characteristics of SBTO(150nm)/ SiO_2(12nm)/Si structure.

voltage was sufficiently improved up to 11 V. Then we measured the C-V characteristics with a voltage sweep of ±9 V as shown in Fig. 9. In this case we also observed a counterclockwise hysteresis loop with a memory window of 0.5 V for reasonably low operation voltages (±9 V). In this sample structure, 2 V out of 9 V can be applied to the SBTO layer. Since the 2Vc estimated the P-E loop for the ±2 V sweep is 0.4 V, the memory window obtained in this work roughly agrees with 2Vc. This suggest the hysteresis obtained in this work is mainly due to the ferroelectric nature of the SBTO films itself.

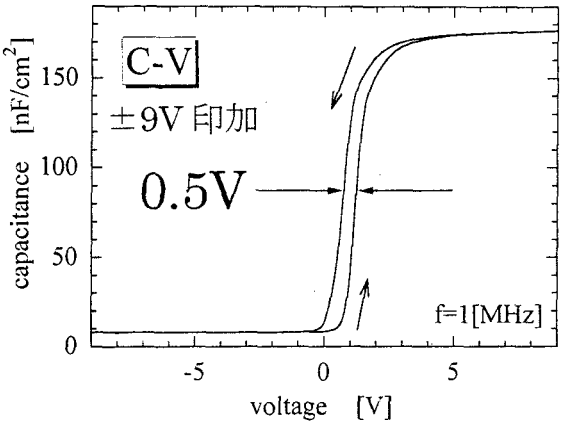

Figure 9 C-V characteristics of SBTO(150nm)/ SiO_2(12nm)/Si structure.

4. SUMMARY

We have demonstrated that $SrBi_2Ta_2O_9$ (SBTO) films can be prepared by the sol-gel technique directly on n-Si(100) substrates. Ploy-crystalline SBTO films were obtained on Si substrates and the crystallite orientations of the film on Si were similar to those of the films prepared on Pt/Ti/SiO_2/Si substrates. SIMS analysis indicated that the inter-diffusion of SBTO and Si was relatively small and that the abrupt interface was obtained even at high annealing temperatures. This is in contrast to the PZT films which strongly diffuses into Si substrates. The C-V plot showed a hysteresis loop with a counterclockwise trace with a memory window of 0.3 V for ±4 V sweep due to the ferroelectric nature of the SBTO films. Furthermore, by inserting the thin thermal oxide between the SBTO films and Si substrates, the breakdown voltage was sufficiently improved. A memory window of 0.5 V was obtained in the C-V measurements when the applied voltages are ±9 V.

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