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Fabrication of Si Single-electron Transistors by Pattern-dependent Oxidation - Oxidation Temperature dependence -

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Oxidation temperature dependence was investigated in fabricating Si single-electron transistors (SETs) by pattern-dependent oxidation, which is the method of converting a narrow Si wire into a nanometer-scale Si island. We have already reported the successful fabrication of SETs at the oxidation temperature of 1000°C ; we tried 1100 and 900°C in this study. SETs fabricated by 1100°C oxidation showed periodic Coulomb blockade oscillations at 25K due to a single Si island which was formed within the Si wire. Device characteristics and their controllability are quite similar to those of 1000°C-oxidized SETs, indicating that the same mechanism of island formation occurs at both 1000 and 1100°C. For 900°C-oxidized devices, the electrical characteristics in the Si wire turned out to be screened by those of additional Si islands which formed at the edges of Si pad layers, to which each end of the Si wire is connected. It was found that these results reasonably agree with transmission electron microscopy (TEM) observations of oxidized Si-wire structures.

Keywords: single-electron transistor, Coulomb blockade, Si wire, thermal oxidation, Si island

1. INTRODUCTION

Thermal oxidation of Si nanostructures has been attracting a lot of attention from the viewpoints of understanding its microscopic physics and its application to Si nanometer-scale devices. We have already reported the fabrication of Si single-electron transistors (SETs) on a silicon-on-insulator (SOI) substrate by pattern-dependent oxidation (PADOX) [1,2]. The method involves the oxidation of a Si wire that runs between two wider pad layers of Si. The initial width and thickness of the Si wire are approximately 30 nm. Since the oxidation reduces the size of the Si wire and converts it into a Si island of 10-nm diameter, the fabricated SET shows the Coulomb blockade oscillation at room temperature. PADOX is useful because we can fabricate various types of single-electron devices by applying it to specially designed patterns [3, 4].

While we used the oxidation temperature of 1000 °C in our previous work, we think that the oxidation temperature is an important parameter in the device fabrication. There have been several reports that show the oxidation-induced strain plays an important role in how the oxidation of Si nanostructures proceeds [5,6]; since the volume expansion with the ratio of 2.25 occurs when Si is changed into SiO_2, the stress is accumulated and significantly retards the oxidation. Then, the oxidation temperature is an important parameter since it affects the viscous flow of SiO_2, which helps to release the accumulated strain [7,8].

Although the successful operation of fabricated SETs indicates that the Si island and two tunnel barriers at both sides are formed within the Si wire, the origin of such an electron potential profile has not yet been clarified. Because the Si island is not surrounded by SiO_2 in all directions and since the Si wire is continuous between the two Si pad layers, we think that the band-gap modulation of Si is responsible for the potential profile. We have so far proposed a model of the Si-island formation, which takes the quantum confinement and the strain into account for the modulation of the Si band-gap [9, 10]. The quantum confinement in the Si wire increased the band-gap, whereas the compressive strain which is expected to accumulate more at the center part of the wire decreased the band-gap. These two effects can lead to the potential well sandwiched by two tunnel barriers.

In this study, we investigated the PADOX-temperature dependence of the electrical characteristics of SETs in order to get a deeper understanding of the role of the strain in Si nanometer-scale devices.

2. DEVICE FABRICATION

Here, we briefly explain the fabrication process [1,2], which is basically similar to the conventional MOS process. The schematic diagram of the device is shown in Fig. 1. We used a SOI substrate with a 400-nm-thick buried SiO_2. A roughly-30-nm-thick superficial Si layer with a 30-nm-thick SiO_2 mask is patterned into a Si wire with pad Si layers by successive electron-beam lithography, reactive

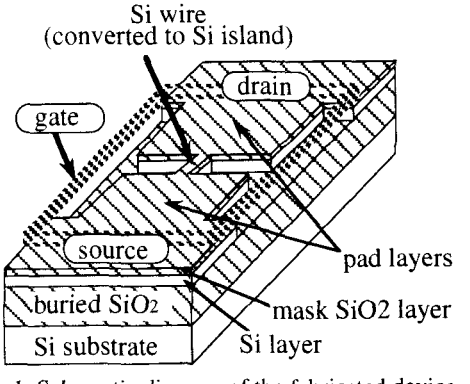

Fig. 1. Schematic diagram of the fabricated device.

ion etching of the SiO_2, and electron-cyclotron-resonance (ECR) plasma etching of the Si. The width and length of the Si wire are 30-50 nm and 30-100 nm, respectively. We used the designed width of 30, 40, and 50 nm, as the parameter of the electron-beam lithography. The lateral width of the Si pad layers to which each end of the wire is connected is typically 400 nm. Then, the wafer is subjected to thermal oxidation in a dry oxygen ambient at temperatures of 900 - 1100°C. For all the temperatures, the oxidation time was so determined that the gate oxide thickness at the two-dimensionally large area would amount to 70 nm, including the SiO_2 mask thickness of 30 nm. The remaining Si was about 10 nm-thick. As a result, the oxidation time was longer for lower temperatures. Typically, they were 300, 80, and 20 minutes for 900, 1000, and 1100°C, respectively. After the PADOX, a phosphorous-doped poly-Si gate was formed to cover a large area. Finally, the source and the drain were formed by the implantation of phosphorous ions using the gate as a mask.

3. ELECTRICAL CHARACTERISTICS OF SET

We measured DC source-drain current (I) of the fabricated devices with an HP4156A. The source and the Si substrate were grounded. The temperature was 24 K.

Devices fabricated by 1100°C-PADOX show electrical characteristics of SETs, which indicate that the self-aligned formation of a Si island occurs at 1100 °C as well as 1000°C. Figure 2 shows source-drain conductance as a function of gate voltage (V_g) for the SET with a 50-nm wide and 100-nm long Si wire. The drain voltage (V_d) was 5 mV. The characteristics show a periodic Coulomb blockade oscillation, which signifies the formation of a single Si island within the Si wire. The more direct evidence is the observation of the so-called Coulomb diamonds. Figure 3 shows a contour plot of the differential conductance ($\partial I/\partial V_d$) as a function of V_g and V_d. It is clearly observed that the current is blocked within the region of successively lying diamonds along the V_g axis at V_d=0 V. From the shape of the diamond, we can estimate the capacitances of the SET; the source, drain, gate, and total capacitances are 0.8, 1.3, 1.5, and 3.6 aF, respectively. The estimated island diameter is 17 nm if we assume the total capacitance to be the self-capacitance of a spherical island.

We have already reported high controllability in the SET fabrication by 1000°C- PADOX [2]. In the detailed study of the Si-size-dependence of the SET characteristics, we showed that the relationship between the gate capacitance (C_g) and the designed length of the Si wire (L) could be expressed as $C_g = A\,(L\text{-}L_{off})$. Here, A is the gate capacitance per unit length and L_{off} is the offset length. Experimentally, A=0.025 aF/nm and L_{off}=26 nm were obtained. This linear dependence strongly indicates that the formation of the Si island occurs by some self-aligning mechanism, and not by random fluctuations of the potential in the Si wire. Figure 4 shows the experimental results on the relation between C_g and L for 1100°C-PADOX SETs. C_g is determined by the measured I-V_g characteristics. The result previously obtained for 1000°C-PADOX is also shown. Although the number of measured devices is not large for

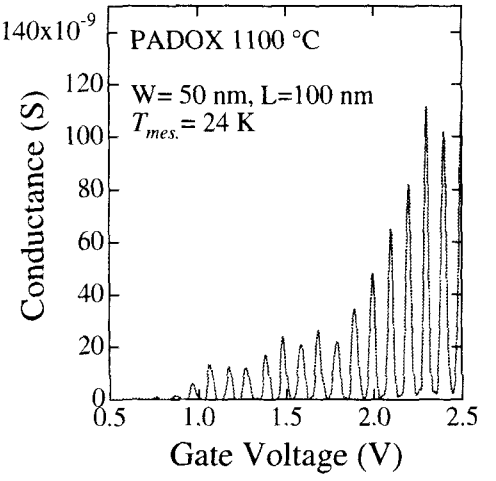

Fig. 2. Source-drain conductance as a function of gate voltage for a SET fabricated by 1100°C PADOX.

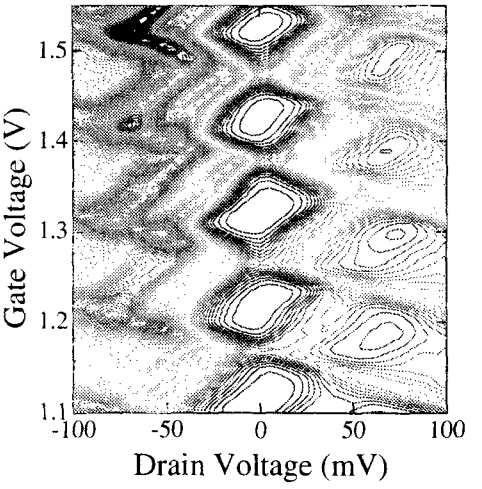

Fig. 3. Contour plot of the differential conductance ($\partial I/\partial V_d$) as a function of V_g and V_d of the 1100°C-PADOX SET.

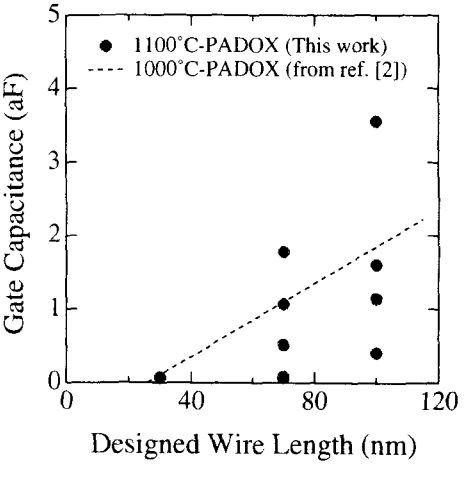

Fig. 4. Relationship between the gate capacitance and the designed wire length of 1100°C-PADOX SETs. Results previously obtained for 1000°C-PADOX SETs are also shown.

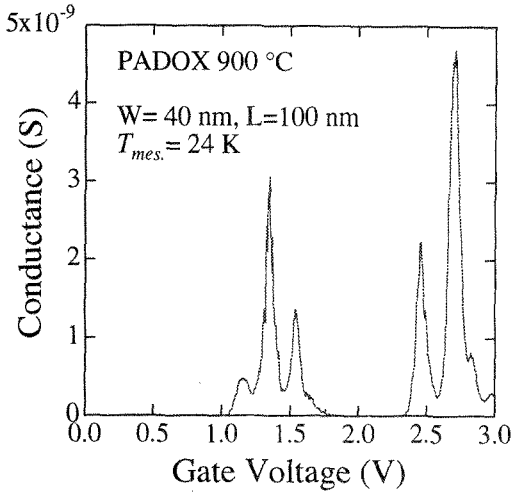

Fig. 5. Source-drain conductance as a function of gate voltage for a device fabricated by 900°C oxidation.

precise discussion, the relations between C_g and L are qualitatively similar for both the temperatures . This suggests that the same mechanism of Si-island formation occurs at both 1000 and 1100°C. If the island-formation model considering the oxidation-induce strain [9, 10] holds true, it also suggests the significant strain and stress accumulates in Si and SiO_2 even at a high temperature of 1100°C. It should be noted that this does not contradict the viscous-flow model of SiO_2 growth [7]. While it is widely known that the release of the stress significantly occurs at temperatures above 1000°C for planar structures such as wafers [8], there have been several reports suggesting the significant retardation of the oxidation in non-planar structures such as Si cylindrical structures [11] in those temperature regions. In the next section, we will show the results of the TEM observations for oxidized Si-wire structures.

Allow me to mention a difference between the 1100°C-PADOX and 1000°C-PADOX. As we noted before, we fabricated devices with designed wire widths of 30, 40, and 50 nm. For the 1000°C-PADOX, good operations of SETs were obtained mainly for the 40-nm wide Si wires. For the 1100°C-PADOX, SETs with 50-nm-wide wires were used since SETs with 40-nm-wide Si wires were not found to be conductive. This indicates that the suppression of the 1100°C-oxidation is less than that of the 1000°C-oxidation due to the smaller viscosity of SiO_2. Then, a part or the whole part of the 40-nm wide Si wire will be completely changed into SiO_2 for the 1100°C-PADOX.

Devices fabricated by 900°C-PADOX also showed electrical characteristics due to the Coulomb blockade. Figure 5 shows source-drain conductance as a function of V_g for a 900°C-oxidized device with 40-nm wide and 100-nm long Si wire. The conductance shows an oscillatory behavior, but rather irregular oscillations. We found that these Coulomb blockade oscillations resulted from unintentionally formed Si islands in the Si pad layers, and not from within the Si wire. As will be shown in a TEM image in the next section, such parasitic islands may be formed at the edge of the Si pad layer, whereas the size of the Si wire is relatively large due to the significant retardation of oxidation at 900°C. Thus, the electrical characteristics in the Si wire can be screened by those of the parasitic Si islands. We also confirmed that the origins of the measured Coulomb blockade oscillation are the parasitic Si islands, and not the Si island in the Si wire, by means of the substrate-voltage analysis [12]; the method takes advantage of the difference in the substrate-voltage-dependence between the electrical characteristics of the Si wire and those of the Si pad layers. These findings for 900°C-PADOX do not mean that the conversion of the Si wire into the Si island is impossible at this temperature, but suggest that Si pad layers should be protected against the unwanted PADOX. The use of SiN mask is one possible solution [12].

4. TEM OBSERVATION

In this section we will show the results of the TEM observation for oxidized Si-wire structures. Though the observed structure is different from the real SET device, it turned out that the observations can be reasonably related to the electrical characteristics of the fabricated SETs.

Figure 6 shows the cross-sectional TEM images of 50 nm-wide Si wires after the oxidation at 900, 1000, and 1100°C, respectively. The oxidation times were the same as those used in SET fabrication. It should be noted that, for all the conditions, the oxide thickness will amount to about 60 nm when applying the oxidation to a planar Si surface. This means that a 50-nm-wide Si wire will be entirely changed into SiO_2 if there is no oxidation-induced strain. As shown in the TEM images, the Si wire remained and the volume of the remaining Si is larger for lower temperatures. That is, the suppression of oxidation is more prominent for lower temperatures, probably due to a less viscous flow of SiO_2. What is more important is that the suppression is still significant at 1100°C, indicating that the accumulation of the strain is not small even at 1100°C.

Figure 7 shows the cross-sectional TEM images of 400

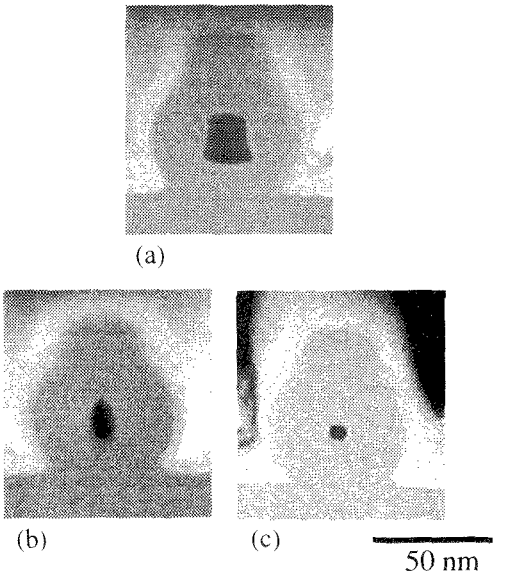

Fig. 6. Cross-sectional TEM images of 50 nm-wide Si wires after the oxidation at (a) 900 (b) 1000, and (c) 1100°C, respectively

nm-wide Si wires after the oxidation at 900, 1000, and 1100°C. As we mentioned before, PADOX significantly occurs even at this relatively wide pattern. There are two basic features involved. One is the oxidation at the Si/buried SiO_2 interface. Hereafter, we will call it the back-interface oxidation. This happens because not only does oxygen reach the Si layer from the surface, but it also diffuses through the opening in the Si pattern and the buried SiO_2 and attacks the back interface from below. Since the density of these oxygen atoms becomes lower as they diffuse far from the pattern-edge due to their consumption at the back interface, the back-interface oxidation is pronounced near the pattern edge. Such a behavior is clearly observed for the 1100°C-oxidized pattern; more back-interface oxidation near the pattern edge results in the higher position of Si because of the volume-expanding growth of SiO_2 at the back interface. The amount of the back-interface oxidation decays as the distance from the patter-edge becomes long. The decay length, in other words, how far the oxygen atoms diffuse towards the center of the pattern through the buried oxide, is determined by the competition between oxygen-diffusivity and reactivity (consumption of oxygen atoms at the back interface). Then, the decay length is expected to be larger for lower temperatures since the temperature dependence of reactivity is larger than that of oxygen diffusivity [13]. Actually, as shown in Fig. 7 (a), an increase in the back-interface oxidation leads to the complete loss of Si at the pattern center for 900°C-oxidation.

The other important feature is the suppression of oxidation at the pattern edge. In Si at the pattern edge, strain likely accumulates because the edge Si is surrounded by the side-wall SiO_2; the situation is similar to the case of the narrow Si wires. Therefore, the oxidation suppression is more prominent for lower temperatures. Consequently, narrow Si wires can be formed at the pattern-edge as shown in Fig. 7 (a). We think that the parasitic Si islands that dominated the electrical characteristics of 900°C-oxidized devices were formed within the Si edge-wire of 400-nm-wide pad layers due to some random fluctuations. We should add that we have recently developed a method of controlling the formation of single Si islands in such Si edge-wires. It was achieved by introducing vertical-thickness modulation in the Si pattern; we call this method the vertical PADOX, or V-PADOX [14].

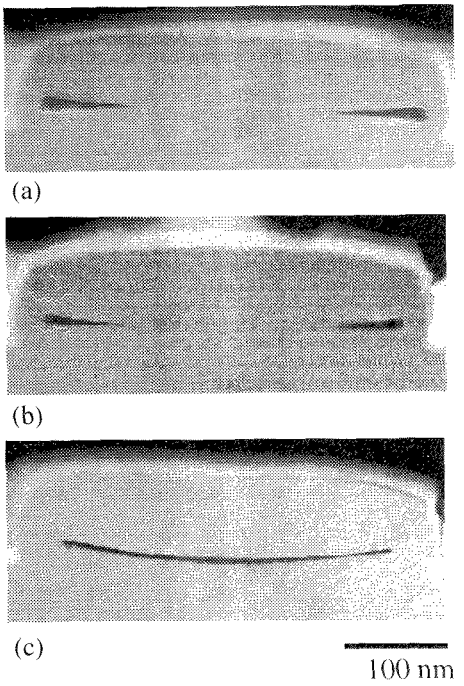

Fig. 7. Cross-sectional TEM images of 400 nm-wide Si patterns after the oxidation at (a) 900 (b) 1000, and (c) 1100°C, respectively

5. SUMMARY

We fabricated Si SETs by PADOX at 1100 °C and 900° C. The devices fabricated by 1100°C-PADOX nicely operated as SETs. Device characteristics are quite similar to those of 1000°C-oxidized SETs, indicating that the same mechanism of island formation occurs at both 1000 and 1100°C. For 900°C-oxidized devices, the electrical characteristics were screened by those of the parasitic Si islands, which are unintentionally formed in the pad layers by PADOX.

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