Transactions of the Materials Research Society of Japan 26 [2] 723-726 (2001)

Single-Electron Memory using Self-Assembled Gold Nano-Particles

Masakazu Baba and Jaw-Shen Tsai
Fundamental Research Laboratories, NEC Corporation, 34 Miyukigaoka, Tsukuba, Ibaraki 305-8501, Japan
FAX: 81-298-56-6139, e-mail: babam@frl.cl.nec.co.jp
Tohru Nakamura
National Institute of Materials and Chemical Research, 1-1 Higashi, Tsukuba 305-8565, Japan

We investigated a memory device that uses self-assembled gold particles as the electron trap node. These particles were connected to each other and to the control electrode by using organic molecules that work as the tunnel junction. We observed the charging and discharging of the multi-tunnel junctions with 10 nm gold particles. The operating temperature was estimated to be about 170 K by plotting the relationship between temperature and retention time. The read-out was carried out by a single-electron transistor.

Key words: single-electron memory, single-electron transistor, gold colloidal particle, organic molecule, Coulomb blockade

1. INTRODUCTION

The so-called single-electron memory (SEM) that takes advantage of the charging effect is a candidate for the future memory devices that require a high integration and a low power consumption. The operating temperature of such single-electron devices is directly determined by the geometrical size of the device. For a room temperature operation, the island size of the device should be less than 10 nm. Such a small size is considered to be less than the fabrication limit of conventional electron beam lithography. Instead of such brute-force physical method, in the fabrication of such nanostructures, the more "bottom-up" approaches that involved self-assemblies of nanometer-sized units were also pursued. Various types of the electron-storage memory nodes have been proposed in single-electron memories, such as self-forming nanocrystals.[1-3] Single-electron circuit normally consists of three components, small conductive island, thin tunnel barrier, and electric leads. Here we report our experiment in which not only the islands, but also the tunnel barriers were attempted to be self-assembled. Gold colloidal particles exhibit good size controllability with well-defined diameter were self- assembled in a one- or two-dimensional array and were simultaneously connected to each other and to the control electrode by using aminosilane and thiol organic molecules that work as the tunnel junction. Similar approaches have been demonstrated to form single-electron transistors, and promising results have been obtained with very small gold particles.[4, 5] In this work, we demonstrated the possibility of such linked gold particle array as the component of a small memory cell, in which the storage of very small number of electrons was only needed to represent one bit of signal. The treatment process was very simple and took a short time to complete. The aluminum single-electron transistor (SET), which works as a highly sensitive read-out electrometer,[6] was combined with the gold-particle memory node to form the memory cell. We demonstrate successful memory operation and a possibility of high-temperature operation.

2. EXPERIMENT

The electrometer used here was an Al/AlO_x SET (Al-SET) formed by a conventional method using electron-beam (EB) mask patterning and the three-angle deposition technique, the details of which are described in the literature.[7] The dot size of the SET was about 20 × 20 nm and the Coulomb blockade energy was about 10 meV at 4 K. For the attached memory node, the fourth electrode was fabricated by gold evaporation in

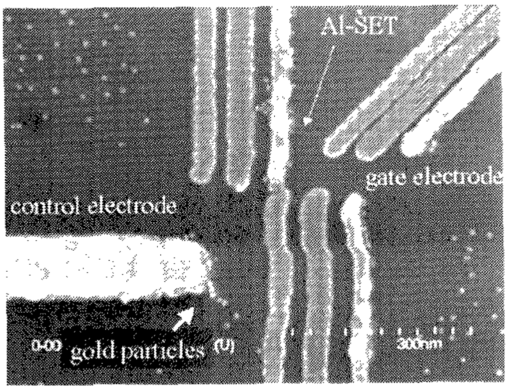

Fig. 1. SEM image of a single-electron memory fabricated from gold nano-particles.

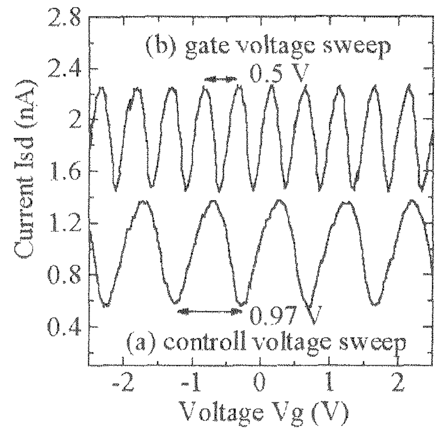

Fig. 2. Current I_{sd} with sweeping (a) V_c and (b) V_g.

the same sequence as used for making the SET-electrode. Since the stencil mask for the SET electrodes was already closed after three aluminum evaporations, the fourth gold evaporation could only make the control-electrode near the Al-SET, as shown in Figure 1. Gold particles selectively attached to the gold electrode as a result of an organic molecule pre-treatment. The substrate (with SET) was cleaned by a brief oxygen plasma ashing (30 s) without breaking the Al-SET junctions. Immediately afterwards, the sample was immersed in a 5 mM ethanol solution of dodecanethiol for 5 min. After the thiol immersion, it was rinsed in ethanol, and dried using a nitrogen gun. Then it was put into aminosilane vapor [3-(2-aminoethylamino) propyltrimethoxysilane, APTMS] for 15 min. This organic-molecule-treated sample was then immersed in a gold colloidal particle solution for 20 min. This procedure provided a submonolayer coating of gold particles (Figure 1). A few gold particles forming a one- or two-dimensional array attached to the gold electrode. Thiol and aminosilane molecules became adhesion agents on the gold electrode, Si-oxide substrate, and each other. One tunneling barrier between the control electrode and a gold particle was the thiol molecules and other among gold particles was pre-coated citrate molecules.[4] This gold nano-particle treatment, immersing samples in organic solution and gold colloid, takes only about one hour, and is an easy fabrication process.

3. RESULTS and DICUSSION

We measured the electrical characteristics of our device in a cryostat. The device was symmetrically voltage-biased between the source and drain at V_B. We used the method described by Chen et al.[8] to detect only the transferred carrier change in the memory node. This is done by sweeping the control bias (V_c) and gate bias (V_g) at the same time with the relation: $V_g = -V_cC_c/C_g$. Here, C_c, C_g is the coupling capacitance between the dot and the control electrode and gate electrode, respectively. Using this condition, the electric field effect of V_g and V_c on the SET dot is kept constant during the sweeps, and one can observe the effect of the charge transfer of into and out of the memory node alone. The current flowing through the source and the drain of the SET (I_{sd}) is recorded as a function of V_c at 4~12 K.

Clear Coulomb blockade oscillations were observed by sweeping either V_g or V_c within the Al-SET, as shown in Fig. 2. From the oscillation periods, C_g and C_c were estimated to be 0.32 and 0.165 aF, respectively.

Figure 3 shows an example of the actual operation of the single-electron memory, showing the current I_{sd} vs. the control bias V_c at 4.2 K. The control bias was increased from 0 V to maximum voltage, and returned to 0 V. The curves are shifted for clarity. At small V_c, although the potential of the memory node was affected by the surrounding gates, the sum induced charge on the island was kept at zero and the current was not modulated. As V_c was brought to greater than a threshold value (V_{th}) of 8 V, the current I_{sd} started to oscillate, indicating that the potential of the memory

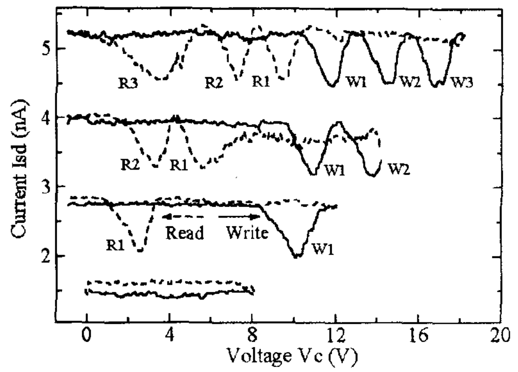

Fig. 3. Current vs. control bias voltage (with a compensation gate bias voltage) for a gradually increased maximum sweep voltage. For clarity, the current in each curve is shifted upward by 0.3 nA. As the voltage increased, the write operation was caused at W1, W2, and W3. As the voltage decreased, on the other hand, the read operation was caused at R1, R2, and R3.

node changed due to a charge in the number of excess electrons in the node. This potential change could no longer be canceled by the gate bias, thus the current showed oscillatory modulation. This modulation was direct evidence of the electron transfer events.

As the control bias voltage was swept from zero to the maximum voltage, the oscillations of W1, W2, and W3 were clearly shown. In addition, as the control bias was swept back to zero, the oscillations of R1, R2, and R3 were shown. The number of oscillation peaks depended on the maximum voltages. At the next voltage sweeping, there was no peaks at lower voltage less than 8 V. When V_c was biased more than 8 V, the charging began and a write operation could be done. After that, when V_c was decreased to zero, the discharging began and a destructive read operation could be done. All these facts confirm the successful operation of the memory device and the effectiveness of gold nano-particles as a memory node.

We also estimated the retention time of the memory by monitoring I_{sd} after sweeping the voltage to the maximum voltage for one or two write peaks, and then back to the threshold voltage V_{th}. The curves in Figure 4 were obtained at 11, 11.5 and 12 K in a device whose threshold voltage was 3 V and whose write voltage was about 10 V. It is clearly seen that current I_{sd} oscillates in time as electrons escape the memory node. The retention time was defined as the time between the top of the final

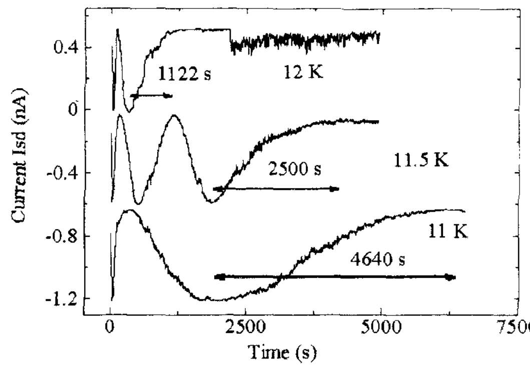

Fig. 4. The dependence of I_{sd} on time after the device is written at 10 V.

peak to the steady state zero level. In Fig. 4, the retention times become 1100, 2500, and 4600 s at temperatures 12, 11.5, and 11 K, respectively. The retention time clearly depends on the temperature.

Figure 5 plots the retention time vs. temperature. It is clearly shown that there is an exponential relationship between retention time and temperature. The slope of the Arrhenius plot gives the apparent thermal activation energy of this memory device. [9] The memory node consist of a few gold nano-particles, so the memory activation energy is the sum of the charging energy between each particle. Although the number of the electron escaped in during the defined retention time, since the succeeding electron escape takes an exponentially longer time to happen compared to the

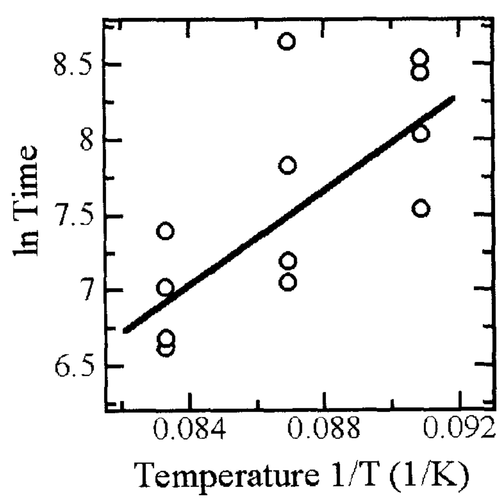

Fig. 5. Arrhenius plot of measured retention time vs. temperature. The slope of this plot gives the thermal activation energy of 15 meV (174 K).

previous escaping event, the activation energy probably is dominated by the last single-electron tunneling event. In most samples, however, the energy becomes about 15 meV. The same number of gold-particles was attached to the gold control electrode through our method. From this energy value, we can estimate the operation temperature of this memory device to be roughly 170 K.

4. CONCLUSION

To summarize, we have described a single-electron memory that utilizes electron traps in a gold nano-particle array as the memory node with organic molecule treatment. Its successful operation was demonstrated in the write/read memory characteristic and the retention time. The operation temperature was around 170 K.

References

[1] K. Yano, T. Ishii, T. Hashimoto, T. Kobayashi, F. Murai, and K. Seki, *IEEE Trans. Electron Devices* **ED-41**, 1628 (1994).

[2] S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbé, and K. Chan, *Appl. Phys. Lett.* **68**, 1377 (1996).

[3] N. Takahashi, H. Ishikuro, and T. Hiramoto, *Appl. Phys. Lett.* **76**, 209 (2000).

[4] T. Sato, H. Ahmed, D. Brown, and B. F. G. Johnson, *J. Appl. Phys.* **82**, 696 (1997).

[5] D. L. Klein, P. L. McEuen, J. E. B. Katari, R. Roth, and A. P. Alivisatos, *Appl. Phys. Lett.* **68**, 2574 (1996).

[6] H. Sunamura, T. Sakamoto, Y. Nakamura, H. Kawaura, J. S. Tsai, and T. Baba, *Appl. Phys. Lett.* **74**, 3555 (1999).

[7] Y. Nakamura, C. D. Chen, and J. S. Tsai, *Jpn. J. Appl. Phys., Part* 2 **35**, L1465 (1996).

[8] C. D. Chen, Y. Nakamura, and J. S. Tsai, *Appl. Phys. Lett.* **71**, 2038 (1997).

[9] P. D. Dresselhaus, L. Ji, S. Han, J. E. Lukens, and K. K. Likharev, *Phys. Rev. Lett.* **72**, 3226 (1994).

(Received December 8, 2000; Accepted December 19, 2000)