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Electric Properties of Nanotube Ring Device Measured with Dual-probe Scanning Tunneling Microscope

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We have constructed dual-probe scanning tunneling microscope (D-STM), where we use carbon nanotubes (NTs) as STM probes. This D-STM allows us to elucidate the electric property of a sample with a spatial resolution of ~10 nm. Using D-STM, we have measured the current-voltage (*I-V*) curves of an NT ring gate Si transistor (gate length ~12 nm), which show that the NT ring behaves as a gate terminal on the Si substrate. Furthermore, we have constructed an NT ring transistor (size ~20 nm) to measure the I-V characteristic for various gate voltages. These results cause that NT ring would be promising material for new type electronic devices.
Key words: carbon nanotube, nanotube ring, STM, transistor

1. INTRODUCTION

The use of individual molecules as functional electric devices has been expected, because it could lead to new technology in the field of electronics industry. Recently, advances in the molecular electronics have resulted in electrical measurements on single molecule of carbon nanotubes (NTs)[1-3] or C_{60}[4]. Especially, NT has been regarded as an ideal material for the molecular electronics. Because individual NTs would act as electric devices such as a diode[5], a field effect transistor (FET)[6] or a single electron transistor[7]. Furthermore, they have been stimulating electric properties such as ballistic transport[8] and Lattinger Liquid[9]. However, the difficulty of wiring and controlling the length of NT remained in order to realize the molecular electronic circuits.

Here we have constructed new method, that is dual-probe scanning tunneling microscope (D-STM), which was composed of two probes and two individual STM systems. D-STM can control positions of two probes in three dimensions on the sample to measure their electric properties with ~10 nm accuracy. Furthermore, we can prepare NT rings[10] of 10-200 nm in diameters for transport wires or gate electrodes for nanometer scale transistor. In this study, we show that the D-STM can allow us to measure electric properties of NT ring as nanometer scale devices.

2. EXPERIMENT

2.1 D-STM system

The difficulty of multi-probe STM[11] lies in the interference between probes. The distance between probes cannot be less than radius of curvature in the apex, because probes collide with each other. This causes that the conventional W or Pt/Ir STM tips cannot be used for D-STM with desired spatial resolution of less than 20 nm, because of their radius of curvature being more than 100 nm by electrochemical etching. In this study, we applied the metallic multi-wall NTs as D-STM probes[12,13].

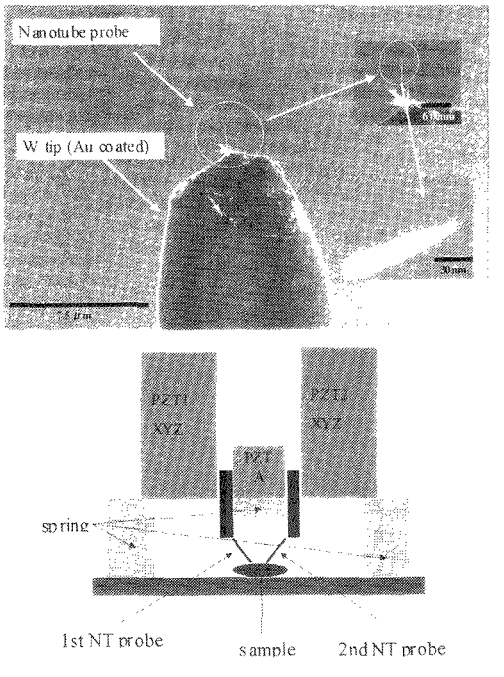

Fig.1. NT probe and D-STM system. (a) SEM images of NT probe for D-STM. The diameter of NT is ~12nm near its apex. (b) Schematic of D-STM and active damper system. First and second PZT are connected with small PZT which can vibrated NT probes to reduce their vibration noise.

Figure 1(a) shows the scanning electron microscope (SEM) image of NT probe, in which multi-wall NTs (diameter < 12 nm) were attached to the apex of a W tip (Au coated). We attached NTs to the W tips with the micro-manipulator system, which has the spatial resolution of less than 0.5 μm.

In our D-STM system, high aspect ratios and small effective radius (<10 nm) of NT probes significantly improve spatial resolution beyond what can be achieved using conventional W tips. However, NT probes of 10-20 nm in diameter can easily bend and vibrate. Therefore, the noise reduction system should be sufficiently powerful to have a stable measurement of the D-STM. We have developed the active damper system, as the noise reduction system for D-STM. Figure 1(b) displays the schematic of our developed D-STM with the active damper system, which is composed of a small piezoelectric actuator (PZT) and a spring. The PZT-A in Fig.1(b) is vibrated at the same frequency of the signal noise with shifting the phase of 180°, so that the mechanical vibration noise can typically decrease from 2-3 nm to less than 0.1 nm. Under operation of the active damper system, the spatial resolution of D-STM achieved to less than 1 nm with scanning two probes simultaneously, while less than 0.1 nm with scanning each NT probes individually.

2.2 NT rings

The controlling the length of NT wires will be effective to provide nanometer scale NT devices. In this study, we controlled the size of NT rings with buoyancy in the solution. Since NTs have a character of the strong van der Waals attraction between tubes, NT rings resulted from the folding of straight single-wall NTs (SWNTs) with ultrasonic irradiation. Purified SWNTs (>99 % in soot) were irradiated with ultrasonic (20 kHz, 50 W) in benzalkonium chloride methanol solution (5%) for 2.5 hours. Then, we found that small size NT rings were organized in the solution with narrow distribution (radii =10-200 nm). Figure 2 shows the STM image (constant current mode) of obtained NT rings. These rings were deposited on the substrate.

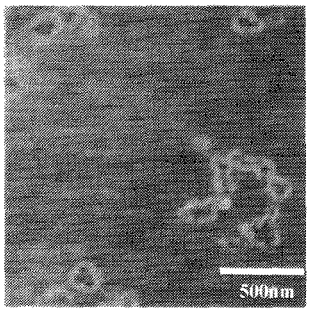

Fig.2. STM image of NT rings.

3. RESULTS AND DISCUSSION

3.1 NT ring gate transistor

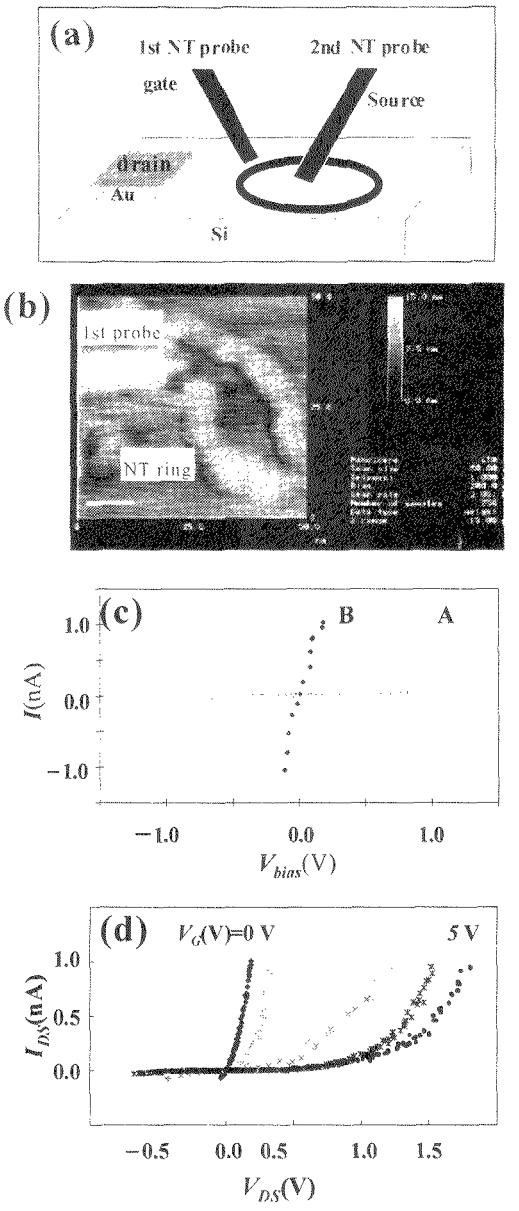

Fig.3. NT ring gate Si transistor. (a) Schematic of configuration of experimental measurement. First NT probe as gate terminal joined with NT ring and second one as source terminal attached Si surface. (b) STM image (constant current mode) of NT ring joined with NT probe, (scale bar, 10nm). (c) The *I-V* (probe current-bias voltage) curves of the NT probe and the substrates. A and B are before and after application of high bias voltage (~15V) between the NT probe and the substrate. (d) *I-V* (I_{DS}-V_{DS}) curves of NT ring gate Si transistor. V_G from left to right are 0, 1, 2, 3, 4 and 5 V, respectively.

Individual NT transistors joined with NT wires could realize fabrication of nanometer scale circuit. Our D-STM permits any single NT ring to connect with two NTs, as functions of the source and drain terminals. Therefore, we will measure current-voltage (*I-V*) characteristic of an NT ring device. In this study, we have measured the characteristic of a Si transistor with an NT ring gate terminal.

The *p*-type single-wall NTs should be gate electrodes on the *n*-type Si layer, since the junction of a doped Si and the NTs is expected to form a Schottky barrier. Hence, we used semiconducting NT rings (*p*-type) as gate electrodes to verify the property of a doped *n*-type Si as a drift layer of a transistor.

Figure 3(a) shows the schematic of this device. In this experiment, we will use NT rings for the gate electrode on the Si substrate. In this terminal configuration, the gate length is ~12 nm, that is the thickness of NT wire of the ring. In order to measure the samples under the atmosphere, we prepared hydrogen-terminated Si substrates. Because the termination of Si dangling bonds by hydrogen atoms can prevent from oxidizing the Si surface. The Au electrode used as a source electrode was embedded at the length of ~100 nm from the NT ring gate.

Figure 3(b) shows the D-STM constant current image of an NT ring (diameter ~50 nm) and the first NT probe. We positioned the first D-STM probe on the NT ring, as shown in the D-STM image (Fig.3(b)) recorded by scanning the second probe. We attached the second probe on the substrate at the center of the NT ring to form the source electrode on going to fix the first probe upon the NT ring of the gate terminal.

In order to form an ohmic contact in the source electrode, we attached the second probe to the substrate and applied high voltage (=15 V) to the second NT probe. After the application of high voltage, the voltage gap dismissed from ~1.2 V to ~0.1 V in the probe current-bias voltage (*I-V*) curve, as shown in Fig.3(c). This result would be attributed to desorption of the terminating hydrogen atoms or other adsorbates from the Si surface. Hence, an ohmic like contact would be formed between the second probe and Si substrate. We can therefore use the second probe as the source electrode and compose an NT ring gate Si transistor.

Figure 3(d) shows the *I-V* curves of this NT ring gate Si transistor for various gate voltages (V_G) at room temperature in the dry nitrogen. There is small increase in current for larger reveres bias than that of NT ring transistor. The *I-V* curves shifted along the source-drain voltage (V_{DS}) axis as a function of V_G. Around V_G=0 V, a small nonlinearity exists in the *I-V* curve. When V_G is increased to positive values, a definite voltage gap grows larger around V_{DS}=0 V and asymmetric structure of *I-V* curve. The current is essentially zero (<0.1 pA) up to a threshold voltage of a few volts. This result shows that the NT ring gate is considerably effective for the formation of carrier depletion in the Si.

In a field effect transistor (FET) of ~10 nm channel length, the electrostatic field induced near the gate can control mainly the carrier drift without the pinch-off region. Therefore, induction static field causes the nonlineality in the *I-V* curve and the switching behavior, and then their *I-V* characteristic may have no saturation region.

3-2. NT ring transistor

A semiconducting NT ring connected with two metallic multi-wall NT wires would have behavior of a transport region of a transistor, that is a NT ring transistor. D-STM can measure the electric properties of NT ring transistor, since D-STM provides two NT probes to position any single NT ring, as shown in Fig.4(a). Figure 4(b) shows a D-STM image of first NT probe attached with an NT ring (diameter: ~10 nm), which was obtained by scanning the second probe. In this experiment, the NT ring was deposited on the ploy-Si/SiO_2/Si(100)/Au substrate, where Au layer acted as a gate terminal (Fig.4(a)).

Figure 4(c) shows the *I-V* characteristic at the room temperature under dry nitrogen for the sample configuration shown in Fig.4(a). From these data, we found that larger current can flow between source and drain terminals in comparison with Si transistor with an NT ring gate. The current density at V_{DS}=1 V and V_G=1 V was calculated to be more than ~10^{10} Am^{-2} (for comparison, the current density for metal superconductors is typically 10^8-10^{10} Am^{-2}). These results can estimate that carriers can flow in the NT ring with ballistic like transversal.

The current density *J* in ballistic transport can be expressed by Child-Langmuir equation[14] of

$$J = (4/9)\varepsilon\varepsilon_0 d^{-2}(2e/m^*)^{1/2}V_p^{3/2},$$

where $\varepsilon, \varepsilon_0$, d, e, m^*, V_p are relative dielectric, constant, dielectric constant in vacuum, distance between source and drain terminals, elementary electric charge, effective mass of hole in NT, and bias voltage between source and drain terminals, respectively. Using the equation with ε=5.5 in graphite, d~30 nm for circumference of a NT ring and m^* ~$0.01m_o$ in semiconducting NTs (m_o: electron mass), we have J=1.4×10^{11} Am^{-2} at V_p=1 V. This calculation value is less than the result of *I-V* characteristic (~10^{10} Am^{-2}). Therefore, at room temperature, the carriers in the NT ring may be slightly scattered to decrease the flow rate of ballistic transversal carriers.

In addition, this device gives a maximum change in V_G from 4 V to 5 V in, so that the estimation of gain results in 0.9. (The gain of this transistor can be estimated from V_{DS} ratio over the NT ring transistor at a certain I_{DS}.) If the gain of these ballistic devices becomes more than unity, we will expect to fabricate the THz switching speed devices using NT rings.

The measurements of the NT ring transistor properties with D-STM show the possibility of NT materials electronics circuits. Especially, D-STM becomes the powerful method for nanometer scale measurements.

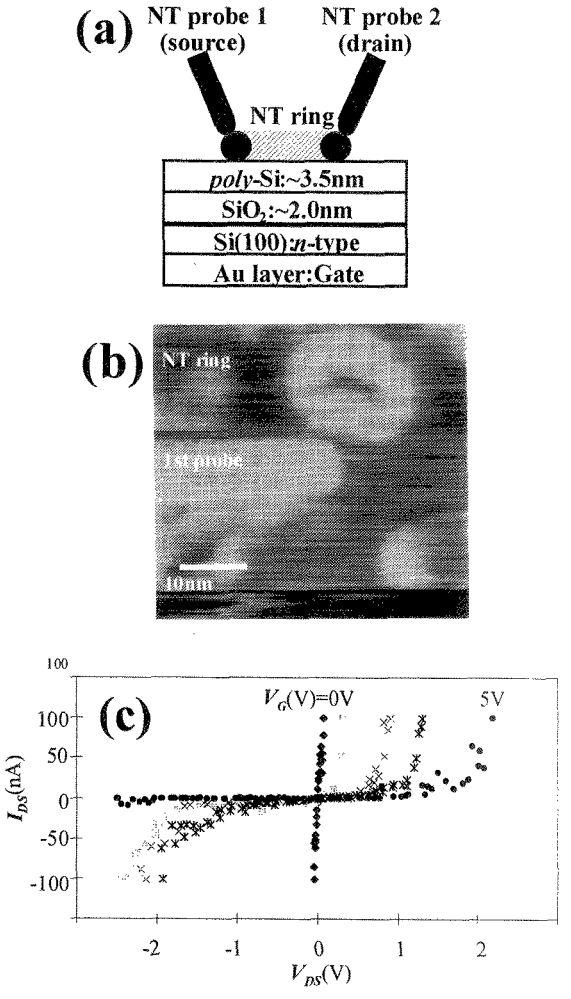

Fig.4. NT ring transistor. (a) Schematic of configuration of experimental measurement. The first NT and second NT probes were connected with a NT ring on the *ploy*-Si(~3.5nm, n-type)/SiO_2(~2.0nm)/Si(100)/ Au substrate, where Au layer acted as a gate terminal. (b) STM image (constant current mode) of NT ring (size ~20nm) joined with NT probe, (scale bar, 10nm). (c) *I-V* (I_{DS}-V_{DS}) curves of NT ring transistor. V_G from left to right are 0, 1, 2, 3, 4 and 5 V, respectively.

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