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Single Electron Transistor Readout of Ferroelectric Memory Capacitor

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Localized polarization response and charge noise have been measured by single electron transistors (SET) made on $PbZr_xTi_{1-x}O_3$ film, which functions as a memory capacitor. Offsets, i.e., the position of the island electrode of the SET, are out of alignment with the Pt-bottom-gate electrode, resulting in a variety of charge noise levels detected by the SET. A maximum charge noise at 5 V of bottom gate voltage was observed for the sample with the island positioned over the edge of the Pt-bottom-gate electrode, where the $PbZr_xTi_{1-x}O_3$ crystallinity was in an intermediate phase between perovskite and pyrochlore, and grain boundaries were not clearly observed. Conversely, a transistor with minimum offset alignment exhibited an increase in the charge noise level with the increasing higher bottom gate voltages up to 7 V. These results indicate that the local polarization is detected near the island electrode of the SET. The threshold gate voltage of about 6 V was deduced from dielectric constants, the thickness of capacitors, and the coercive field of $PbZr_xTi_{1-x}O_3$. This expected threshold of "write" operation was confirmed in the latter transistor. A memory operation was thus successfully demonstrated.

Keywords: SET, $PbZr_xTi_{1-x}O_3$, perovskite, pyrochlore, memory, polarization

1. INTRODUCTION

Single-electron transistor (SET) memories [1-3] with less than 10-nm sizes are expected to realize much larger integration levels and much lower power consumption than current commercially available memory devices. A specific application of SET as an electrometer has already demonstrated current measurements in a unit of e/2 for appropriate bias conditions [4].

Conversely, ferroelectric materials used in memory devices must have non-volatile characteristics, high-speed response, low power consumption, and long endurance times. These advantages have been demonstrated in current Ferroelectric Random Access Memory (FeRAM) [5]. The fatigue [6] found in $PbZr_xTi_{1-x}O_3$ (PZT) was resolved by using $SrBi_2Ta_2O_9$ (SBT), which brought FeRAM to the market. Successful FeRAM fabrication, however, requires a new scaling effect to further miniaturize the memory capacitor. Scanning force microscopy (SFM) observation of ferroelectric film [7] has been proposed to maintain a highly uniform capacitor size/grain size ratio in less than sub-μm^2 capacitors. However, in actual nanoscale devices, crystallinity, grain sizes, charge behavior, and their related problems have not been studied. This study is a new approach for observing charge behavior of the PZT film by using a highly sensitive SET electrometer. We will discuss the localized polarizations on the PZT. Crystallinity and/or grain size variations will be detected through the electronic properties of SETs on the PZT capacitor that have different alignments of the island electrode of the SET with the Pt-bottom-gate electrode.

2. DESIGN AND FABRICATION OF THE SAMPLES

The device structure, as shown in Fig. 1, consists of a metallic junction SET as an electrometer using a PZT capacitor. A ~25 nm metal-dot island in a SET component is aligned on the SiO_2/PZT/Pt layer. To build up an SET on a memory node capacitor [3] requires a much larger integration level compared with other SETs fabricated in planer configurations [1-2]. The SET readout part,

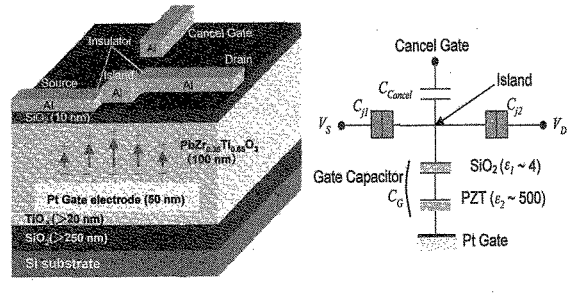

Fig. 1 Device structure (left) and equivalent circuit (right).

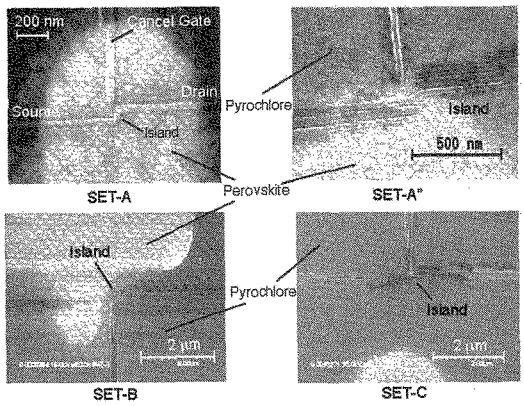

Fig. 2 SEM images of samples: SET-A (top left), SET-A" (top right), SET-B (bottom left) and SET-C (bottom right).

combined with the ferroelectric capactitor, is a new proposal for producing stress-free memory processes with high-speed response compared with Fowler-Nordheim (FN) electron emission in silicon-based SET memories [1] and in metallic junction SETs [2-3]. The SET is screened from the high dielectric constant (ε_2) of ~500 in PZT by the dielectric constant (ε_1) of ~4 in the SiO_2 layer. This screening is expected to avoid decreasing SET operating temperature, which is controlled by the relation $k_BT<e^2/2C$, where k_B is the Boltzman constant, T the operation temperature, e the electron charge, and C the total capacitance of the island. The thicknesses (d_1, d_2) of the SiO_2/PZT layer were designed to suppress the gate voltage V_g given by the relation

$$\begin{aligned} V_g &= V_1 + V_2 = V_2 (V_1 / V_2 + 1) \\ &= E_c d_2 (\varepsilon_2 d_1 / \varepsilon_1 d_2 + 1) \\ &= E_c (\varepsilon_2 d_1 / \varepsilon_1 + d_2), \end{aligned} \qquad (1)$$

where E_c = the coercive electric field.

Gate voltage V_g applied through capacitors C_1 and C_2 should exceed a minimum potential necessary for polarization in the PZT layer. The minimum potential is estimated by assuming that the E_c of the PZT is ~50 kV/cm. The condition for this is $V_2 > E_c \times d_2$. Considering the condition of $\varepsilon_2 \gg \varepsilon_1$ in relation (1), a thinner d_1 is much more preferable than d_2. However, it is the required minimum thickness because of the surface flatness limitations on the film growth [8]. The minimum d_1 (d_2) were more than 10 nm (100 nm) in conventional processes. We therefore selected a 10 nm/100 nm thickness combination of SiO_2/PZT, which will give a switching threshold voltage (V_{th}) of 6.8 V, estimated from relation (1).

Pt was evaporated onto the SiO_2/Si substrate to form the bottom-gate electrode with a thickness of 50 nm. A sol-gel technique was used to form the PZT layer, which was subsequently crystallized by thermal annealing at 450°C for 30 min. The screening layer of 10 nm-thick SiO_2 was deposited by ECR-CVD [8]. Finally, the aluminum SETs were fabricated by a three-angle evaporation technique [9] followed by e-beam lithography and dry etching. All measurements were conducted with an SET source-drain current of 4.0 mV and a temperature of 3 K. PZT polarization at low temperature is possible since hysteresis loops have been measured from 30 K to 290 K by a conventional Sawyer-Tower circuit. The E_c of 56 kV/cm and ε_2 of 440 were obtained at 30 K, which then is potentially possible at 3 K, extrapolating from the temperature dependence.

Figure 2 depicts SEM images of four samples, SET-A to SET-C, which have different alignments of the island electrode from the center of the PZT film capacitor on a Pt-gate electrode. A grain size distribution due to crystallinity differences between the perovskite PZT phase grown on a flat electrode and the pyrochlore PZT phase grown on a SiO2/Si substrate are observed in the SEM images, as already reported in sol-gel derived PZT thin films [10].

3. RESULTS AND DISCUSSION

PZT gate modulation curves for SET-A to SET-C are presented in Fig. 3. The irregular noise coincides with the periodic modulation curve for SET-B: Figure 3 (c) differs noticeably from Figs. 3 (a) and (b). To clarify the charge noise differences, we measured the source-drain current for 10 min as shown in Fig. 4 (a) to Fig. 4 (d), and plotted the noise spectra in Fig. 5. The variety of charge noise levels depends on offset alignments,

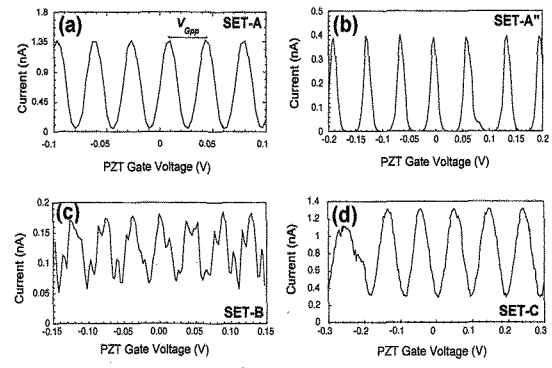

Fig. 3 PZT gate modulation curves at 3 K, 4 mV of source-drain bias voltage.

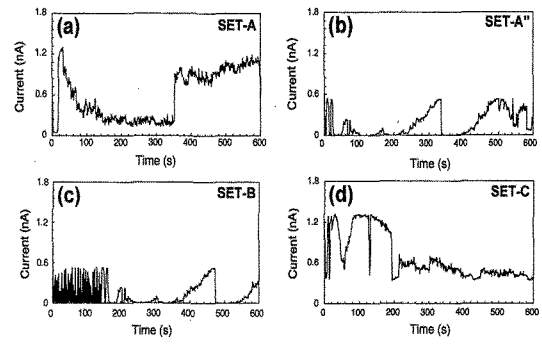

Fig. 4 Source-drain currents for 10 min at 3K, 5 V of PZT gate voltage.

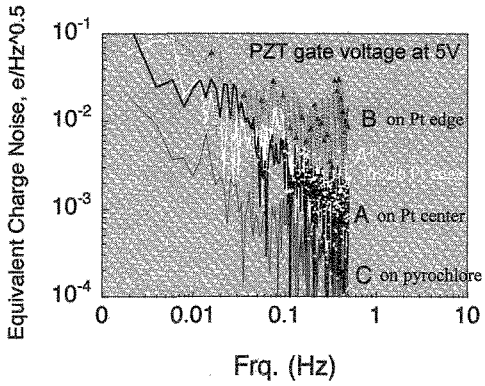

Fig. 5 Equivalent charge noise spectra for SET-A (black lines), SET-A" (white dots with lines), SET-B (dark gray triangles with broken lines) and SET-C (gray lines). PZT gate voltage at 5 V and temperature at 3K.

where displacements are 200 nm (SET-A") up to 2 μm (SET-C) from the minimum offset (SET-A). Thus, SETs detect localized charge response with a resolution of less than 200 nm^2 (Fig. 2). The lowest current noise at gate voltages up to 7 V was obtained for SET-C on pyrochlore PZT, which is offset from the Pt-gate center. In contrast, a maximum charge noise at 5 V was observed for the SET-B primarily because SET-B was aligned over the transitional phase of the PZT crystal, whereas the PZT-crystallinity phase/grain sizes change from perovskite/sub-μm^2 to pyrochlore/~few 10 nm^2. The dielectric constant of ~440 for perovskite is ten-times larger than that for the pyrochlore phase. This greatly strains the electric fields around the Pt-gate edge.

Figure 6 illustrates equivalent charge noise at 0.5Hz as a function of PZT-gate voltages up to 7 V. SET-A, a transistor with minimum offset alignment, demonstrates that the charge noise level increases with higher gate voltages up to 7 V in Fig. 6. This indicates that the local polarizations of PZT grains were effectively induced in the vicinity of the island electrode, and they are expected to be in writing memory operation due to PZT polarization at around 7 V.

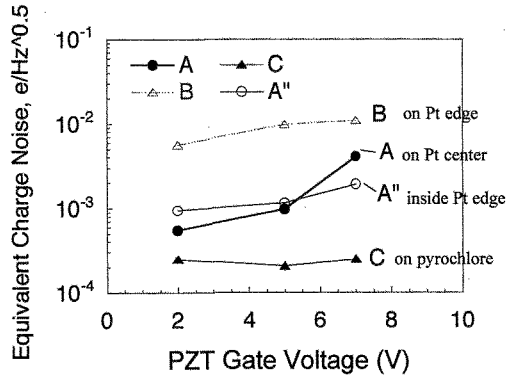

Fig. 6 Equivalent charge noises at 0.5 Hz as a function of PZT gate voltages for SET-A (closed circles), SET-A" (open circles), SET-B (open triangles) and SET-C (closed triangles).

We verified memory operations as follows: By controlling PZT gate and cancel gate voltages in an SET, an oscillatory current modulation period can be matched to one electron charge/discharge in the memory node [2]. Applying a negative voltage V_{cancel} (= $-V_G\ C_G\ /\ C_{cancel}$) keeps the memory node potential constant. Thus, write/erase memory operation can be observed as a modulation period by transferring electrons one by one. The cancel operation factor γ (= C_G / C_{cancel}) was found to be about 77 from the peak-to-peak voltage ratio (=V_{Cpp} / V_{Gpp}) in modulation curves (Fig. 3(a)).

To realize cancellation conditions in our SET, this means V_{cancel} needs to be less than -77 times V_{th} (=6.8 V) to cause PZT polarization. Applying DC offsets just for the PZT gate voltage of V'_G (=V_G + V_{DC}), however, cancels operations that were possible in the practical use range of V_{cancel} = $\pm V_G\gamma = \pm 0.1\gamma$. The writing phenomena in the cancel operations were found to exceed 7 V of V_{DC} as shown in Fig. 7. The writing number of peaks plotted as a function of V_{DC} in Fig. 8 was consistent with the switching threshold voltage V_{th} (=6.8 V) estimated above. The increase of the

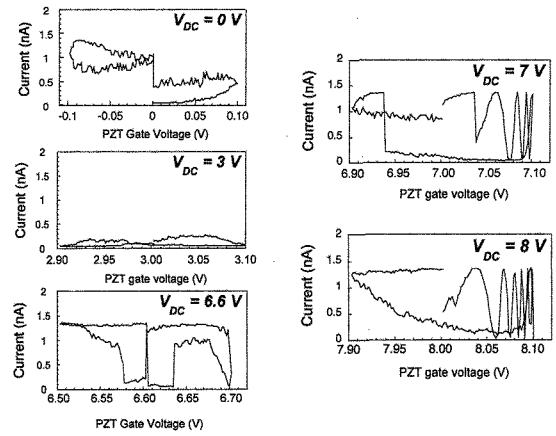

Fig. 7 Writing operation for SET-A under cancellation conditions. DC offsets up to 8 V were applied for PZT gate voltages. The writing threshold voltage of ~ 7 V.

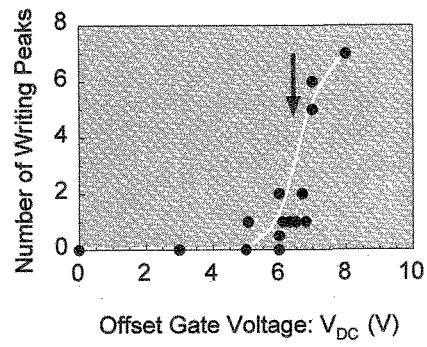

Fig. 8 The writing number of peaks as a function of DC offset for PZT gate voltages. The arrow means the writing threshold gate voltage.

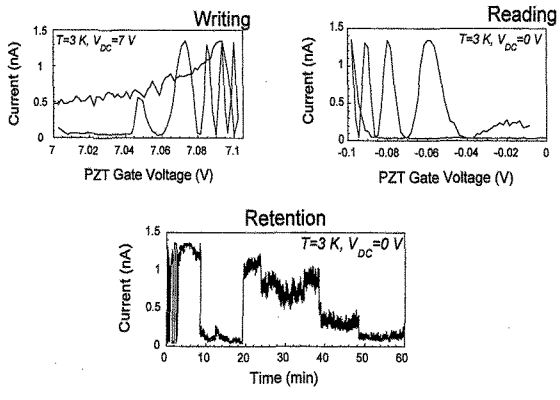

Fig. 9 Wrting waveform at 7 V of DC offset for PZT gate voltage (top left), source-drain current for 1 hour as a retention performance (bottom) and reading wave form at 0 V (top right).

writing peaks simulates a part of a typical Q-V hysteresis loop for the PZT capacitor. The writing waveform at V_{DC}=7 V with cancel operation, time dependence of SET current, and reading waveform at V_{DC} =0 V with cancel operation are shown in Fig. 9. Unwanted rapid switching was observed within 1 hour, which was thought to be a localized polarization originating from PZT grains, or other unstable charge traps in SiO_2 around an island electrode of the SET. Write/read operation corresponded to 5/3 peaks in Fig. 9, which means two peaks were lost within 1 hour due to unknown factors. In spite of a random variation in the time response, the present ferroelectric SET memory successfully demonstrated write/read performance.

4. CONCLUSION

We have presented the first SET readout of PZT polarizations with a resolution of less than 200 nm^2. PZT crystallinity deviation (i.e., transformation from perovskite on a Pt electrode to pyrochlore on a SiO_2 substrate [10]), variations of PZT grain sizes, and strained electric fields have enhanced random charge noise. We have also revealed problems expected in nanoscale, nonvolatile memory devices using ferroelectric materials in the future. An exact SET readout on the perovskite PZT capacitor successfully demonstrated a memory performance. The writing threshold voltage at 6 to 7 V was consistent with a preliminary estimated voltage .

Acknowledgments

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References

[1] A. Nakajima, T. Futatsugi, K. Kosemura, T. Fukano, and N. Yokoyama, Tech. Dig. Int. Electron Devices Meet., 952 (1996); L. Guo, E. Leobandung, and S. Y. Chou, *ibid*, 955 (1996); S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbe, and K. Chan., Appl. Phys. Lett. 68, 1377 (1996).

[2] C. D. Chen, Y. Nakamura, and J. S. Tsai, Appl. Phys. Lett. 71, 2038 (1997).

[3] H. Sunamura, T. Sakamoto, Y,.Nakamura, J. S. Tsai, and T. Baba, Appl. Phys. Lett. 74, 3555 (1999).

[4] L. S. Kuzmin, P. Delsing, T. Claeson, and, K. K. Likharev, Phys. Rev. Lett. 62, 2539 (1989).

[5] S. S. Eaton, D. B. Butler, M. Parris, D. Wilson, and H. McNeillie, ISSCC Dig. of Tech. Papers., 130 (1988); H. Koike, T. Otsuki, T. Kimura, M. Fukuma, Y. Hayashi, Y. Maejima, K. Amanuma, N. Tanabe, T. Matsuki, S. Saito, T. Takeuchi, S. Kobayashi, T. Kunio, T. Hase, Y. Miyasaka, N. Shohata, and M. Takeda, *ibid.*, 368 (1996).

[6] C. A. Paz de Araujo, J. D. Cuchiaro, L.D. McMillan, M. C. Scott, and J. F. Scott, Nature 374, 12 (1995); A. L. Kholkin, E. L. Colla, A. K. Tagantsev, D. V. Taylor, and N. Setter, Appl. Phys. Lett. 68, 2577 (1996): D. Wi, A. Li, H. Ling, T. Yu, Z. Liu, and N. Ming, Appl. Phys. Lett. 76, 2208 (2000).

[7] A. Gruverman, Appl. Phys. Lett. 75, 1452 (1999).

[8] ECR-CVD: Surface roughnesses were less than 1 nm in 2 inch wafer. Technical commnets from NTT-Advanced Technology Co' ltd.

[9] Y. Nakamura, C. D. Chen, and J. S. Tsai, Jpn. J. Appl. Phys., Part 2 35, L1465 (1996).

[10] C. K. Kwok and S. B. Desu, Appl. Phys. Lett. 60, 1430 (1992).

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