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DETERMINATION OF PARAMETERS TO CONTROL ELECTRICAL RESISTIVITIES OF NANO-SCALE COPPER INTERCONNECTS

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In order to determine a key factor to control resistivities of nano-scale Cu interconnects, the resistivities in the Cu interconnects with various line widths (100 nm ~ 1400 nm) were measured using a focused ion beam technique. Single-crystal Cu interconnects were successfully fabricated by etching giant grained Cu films which were prepared by a strain enhanced grain growth technique. The measured resistivities of the Cu interconnects were analyzed using the Mayadas-Shatzkes (M-S) model and the scattering factors by surface and grain boundary were experimentally determined. Our experimental results suggested that the grain boundary scattering was the primary factor which controls the resistivity in the Cu thin films. Using M-S model, we calculated the effective resistivity of sub-100 nm Cu damascene interconnects with various grain sizes, line widths and diffusion barrier thicknesses, and concluded that large grained Cu interconnects and ultra-thin barrier layers were essential to realize the next generation Si-devices.

Key words: Si-devices, copper interconnects, grain growth, thin films, electrical resistivity

1. INTRODUCTION

Copper is attractive as interconnect materials of current Si-ULSI (Ultra-Large Scale Integrated) devices with line width of ~ 130 nm. The advantages of using copper (over conventional Al-alloy) as the interconnect materials are the lower electrical resistivity and higher reliability. However, we have concern to use the Cu interconnects in the sub-50 nm devices, because the resistivity of Cu interconnects increased rapidly by reducing the line width[1-3]. The reason was believed to be due to the relatively long mean free path (~39 nm) of the conducting electrons in copper. Upon reducing the line width of the Cu interconnects down to less than 100 nm, the mean free path of the conducting electrons in copper approaches to the line width, and the electron scatterings by the surfaces/interfaces and/or the grain boundaries would induce drastic resistivity increase. A device designer requires the interconnect resistivity of less than 4 μΩ-cm to realize high-speed ULSI devices with the 70 nm wide interconnects.

It is well known that the electrical resistivity of a thin metal film increases with decreasing the film thickness. This "size effect" on the thin film resistivity has been extensively discussed by Fuchs and Sondheimer and called as the F-S model[4,5]. The resistivity increase due to the surface scattering is explained described by the specularity coefficient P, which is a fraction of the incident electrons that scattered specularly at the surface. Complete specular scattering (P=1) corresponds to no increase in the film resistivity, whereas diffuse scattering (P=0) corresponds to the maximum increase in the film resistivity. However, the resistivity in metal thin films was observed to be larger than the value calculated by the F-S model assuming P=0. Mayadas and Shatzkes (M-S) pointed out that grain boundaries in the films contributed to increase the resistivity in addition to the size effect by the surfaces[6]. Since reduction of the film thickness increase the grain boundary density in the film, the grain boundary scattering becomes dominant for the extremely thin film. In the M-S model, the contribution of the grain boundary scattering expressed by the reflection coefficient R ($0<R<1$) and average grain size. A large R value and small grain size cause significant increase in the film resistivity. Using the combined F-S and M-S model, the resistivities of thin films with various thickness and grain sizes can be calculated if the scattering parameters of P and R are determined. However, there are large variations among the reported P and R values in the Cu thin films.

Recently, the resistivities of sub-0.1 μm Cu interconnects were reported by several authors. Kuan *et al.* fabricated the Cu damascene interconnects with line width of 50 nm using the e-beam lithography, ionized sputtering technique and chemical mechanical polishing processes[1]. They reported that the 50 nm wide damascene Cu interconnects had quite large resistivity ranging from 7 to 13 μΩ-cm. Steinlesberger *et al.* measured the resistivities of Cu interconnects with line width down to 43 nm, which were fabricated by the Cu electroplating technique using the conventional damascene Cu processes with sputtered Ta-based barriers[2]. They concluded that the experimental results agreed very well with the resistivities predicted by the F-S/M-S combined model with P=0.5 and R=0.45. Hinode *et al.* measured the resistivities in fine Cu lines down to 60 nm prepared by electroplating Cu on sputtered Cu seed layers with Ta/TaN barriers[3]. They concluded that grain sizes in the Cu interconnects were sufficiently large so that the grain boundaries did not contribute the resistivity increase, and that the resistivity increase in the interconnects was explained well by the F-S model assuming P=0. It is considered that the differences

among these experimental results are due to difficulties to separate the surface scattering effect from the grain boundary scattering effect using poly-crystalline Cu damascene interconnects which involves inaccuracy of measuring dimensions of the interconnects, thickness of the barrier layers and average grain size.

The purposes of the present investigation are twofold. The first is to prepare a giant grained Cu thin film to fabricate single-crystal Cu interconnects. The second is to determine the parameters which control surface and grain boundary scatterings of the electrical resistivity in the Cu interconnects. Finally, based on these results we will determine the critical resistivity allowed for deep sub-micron Cu interconnects. These studies will provide us a guideline for developing the ultra-narrow Cu interconnects which would be used in the future ULSI devices.

2. EXPERIMENTAL PROCEDURES

The $Si/SiO_2/Si_3N_4$ wafers or rocksalt were used as the substrates in the present experiments. In some cases, prior to the Cu deposition the substrates were deposited by 100 nm-thick TiN layers which are conventionally used as a diffusion barrier layer. The Cu films with various thicknesses (0.1 ~ 3 μm) were deposited onto the substrates at ambient temperatures in the radio frequency (RF) or direct current (DC) magnetron sputtering system. The base pressure of the vacuum chamber was 5.3×10^{-6} Pa. These samples were annealed at room temperature in air and/or annealed at 623 K in Ar or in 5 % H_2/N_2 mixed gas ambient for 2.5 hours. Fine interconnect patterns with length of 10 μm and line widths ranging from 100 to 1400 nm were fabricated in these samples by the focused ion beam (FIB) system. The electrical resistance in the interconnects were measured by a four-point probe method. Microstructural analysis was carried out by using transmission electron microscope (TEM) and scanning ion microscope (SIM) in the FIB system.

3. RESULTS AND DISCUSSION

3.1 Preparation of large grained Cu films

Large grained Cu films were prepared by a strain enhanced grain growth technique, and the fabrication process is briefly reviewed here. The effect of the rigid substrate on the grain growth was previously observed in sputtered Cu films during room temperature storage[7]. The grain growth rates of the Cu films with or without the substrates were measured in the present experiment. As shown in Fig. 1(a), the Cu films deposited on the rocksalt substrates have fine-grained structure after 3 hours storage at room temperature. During room temperature storage, significant grain growth occurs in the Cu film with the rocksalt substrate (Fig. 1(b)). However, when the Cu films are removed from the substrate and stored at room temperature, the grain growth rate become extremely slow and no abnormal grain growth occurs even after 168 hours at room temperature storage (Fig. 1(c)). These results clearly indicate that the room temperature grain growth in the Cu thin films is enhanced by the existence of the rigid substrates, suggesting intrinsic strain (or stress) in the films is the primary factor to control the abnormal grain growth during room temperature storage.

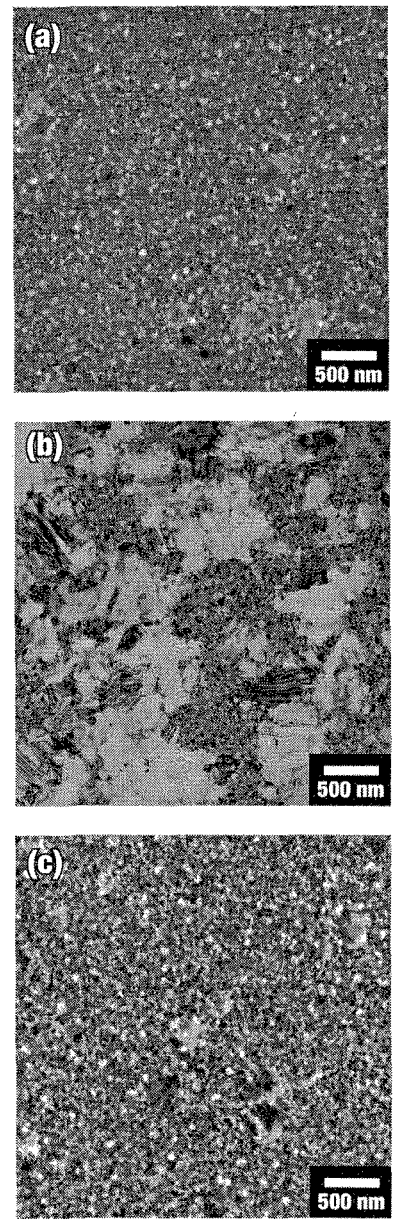

Figure 1 Plan-view TEM image of the 100 nm-thick sputtered Cu film deposited on the rocksalt substrate, annealed at 298 K for (a) 3 h, (b) 264 h, or (c) 192 h without substrate.

The effect of intrinsic strain (or stress) on the grain growth in thick Cu films on the rigid substrates was also studied previously by FIB system[8]. Figures 2(a) and 2(b) repeat the previous experiment and show cross-sectional SIM images of the 3 μm-thick Cu film with the Si/Si_3N_4 substrate. As shown in Fig. 2(a), the 3 μm-thick Cu film after 4 hours storage at room temperature are composed of two layers: large grains (0.3 ~ 0.6 μm) at the bottom, and small grains (~0.1 μm) at the top. The thickness of the large grained layer is about 0.8 μm. After 72 hours storage at room temperature, these large grains at the bottom of the film grow toward the surface of the film. The thickness of the large grained layer is about 1.5 μm and the mean grain size is about 1 μm, while the small grains at the top of the film are stable

(Fig. 2(b)). This clear gradient of grain size in the 3 μm-thick Cu film can be explained by non-uniform strain distribution in the film. Strain and stress in the films are generally induced from the substrate and non-uniform strain distribution was observed for blanket films in direction normal to the substrate surface[9]. An exponential strain distribution normal to the film surface was observed in Pb thin films[10]. The large strain close to the substrate can enhance the growth of the grains located at the bottom of the film. When the film thickness is large, the strain close to the top film surface is relaxed. Therefore, as the film thickness increases, the grain growth rate becomes extremely slow.

These experimental results clearly indicate that strain introduced from the substrate and strain relaxation mechanisms are the primary factors to control the grain growth in the Cu films. Therefore, the interface between the substrates (or the barrier layers) and the Cu films has an important role to control grain growth behaviors in the Cu films.

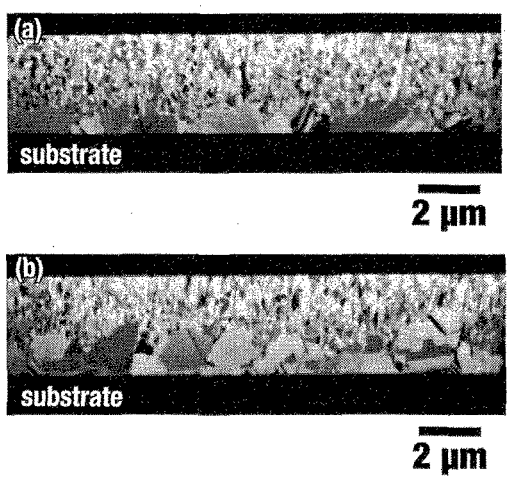

Figure 2 Cross-sectional SIM image of the sputtered Cu film on the Si_3N_4 substrate, annealed at 298 K for (a) 4h or (b) 72h

3.2 Resistivity measurements of Cu interconnects fabricated by FIB technique

Based on the technique described in the previous section, grain sizes of the sputtered Cu films were increased by depositing the TiN adhesive layers and we successfully prepared giant grains of around 5~10 μm. Although the average grain size in the sputtered Cu thin films is larger by a factor of ~ 5 than the film thickness even after annealing at elevated temperatures. The average grain size was ten times larger than the film thickness when the strain enhanced grain growth technique was applied. Using the giant grained Cu films, interconnect patterns for resistivity measurements were fabricated by the FIB technique as shown in Fig.3. This technique enabled us to fabricate the interconnect patterns selectively within a giant grain. SIM observations showed that the Cu interconnect pattern has very smooth sidewalls and that there are no grain boundaries except a few twin boundaries. Thus, we treat such interconnects as "single-crystal" Cu interconnects.

Figure 4 shows correlation between the measured

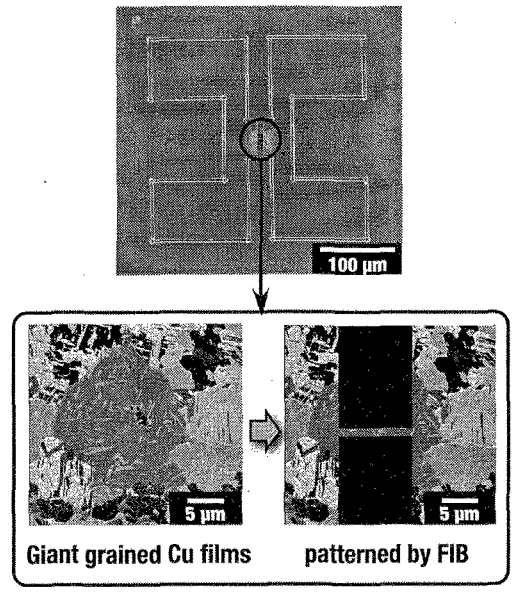

Figure 3 Interconnect pattern for resistivity measurement, which was patterned in a giant grained Cu films by FIB technique.

resistivities and the line width of the single-crystal Cu interconnects. The resistivities increase with decreasing the line width. The resistivity of the single-crystal Cu interconnects with line width of 100 nm is about 2.1 μΩ-cm. Since these single-crystal interconnects have no grain boundaries, the effect of grain boundary scattering can be neglected and the resistivity increase could be attributed to the surface and interface scattering. Comparing the theoretical values and the experimental data of Fig.4, the P value was determined to be zero, which corresponds to the maximum increase of the resistivity by the surface scattering. The resistivity of interconnects with line width of 65 nm is estimated to be approximately 2.5 μΩ-cm from the extrapolated curve, if there is no grain boundary in the interconnects.

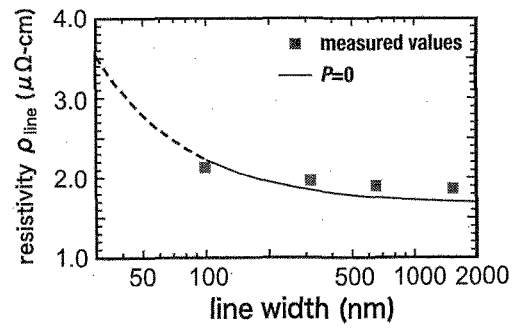

Figure 4 Measured resistivity of single-crystal Cu interconnects as a function of line width

In order to study the effect of grain boundaries on the resistivities in Cu interconnects, the Cu thin films with various grain sizes were prepared by the sputtering technique and patterned by the FIB technique. Figure 5

shows correlation between the measured resistivity in the poly-crystal Cu interconnects with grain size of 700 nm and the line width. Using the M-S model, the scattering coefficient R can be determined to be 0.45 using P=0, which was determined by the experimental results for the single-crystal Cu interconnects.

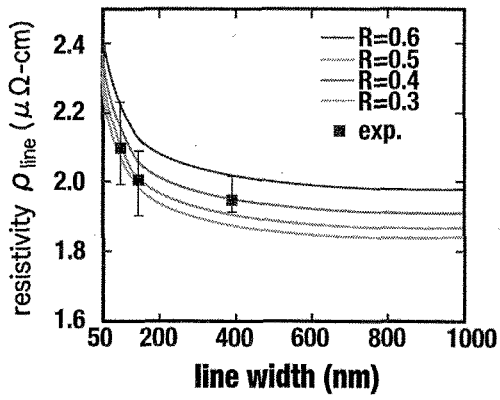

Figure 5 Resistivity of poly-crystal Cu interconnects which have mean grain size of 700 nm as a function of line width.

3.4 Effective resistivity of nano-scale Cu interconnects with barrier layers

For the manufacturing damascene Cu interconnects the diffusion barrier layers are needed to prevent intermixing of copper with the surrounding dielectric materials. The existence of the barrier layers reduces the cross-sectional area of copper, and effective resistivity of the interconnects become larger than the barrier-free Cu interconnects. The effective resistivity in nano-scale Cu interconnects with barrier layers was calculated using the values of P=0 and R=0.45. The resistivities in barrier-free single crystal Cu interconnect with line width of 65 nm and 45 nm are approximately 2.3 μΩ-cm and 2.7 μΩ-cm, respectively. These values are smaller than the value of 4 μΩ-cm. However, when the barrier layer with thickness of about 10nm are deposited in the damascene structure, the net interconnect resistivity would exceed the value of 4 μΩ-cm even in single crystal Cu interconnects. In the case of 45 nm wide poly-crystal Cu interconnects, the effective resistivity is close to that of barrier-free Cu interconnects. This calculation suggests that a very large grain size and an ultra-thin barrier layer should be developed to reduce further the electrical resistivity of the nano-scale Cu interconnects.

4. SUMMARY

Single-crystal Cu interconnects were successfully fabricated within a giant grained Cu films which were prepared by a strain enhanced grain growth technique. Comparing the theoretical values and the measured resistivities in single crystal Cu interconnects, the P value was determined to be zero, which corresponds to maximum increase of the resistivity by surface scattering. Using the M-S model which correlates the electric conduction in thin films with grain size and film thickness, the grain boundary scattering coefficient R was estimated to be 0.45. Our experimental results

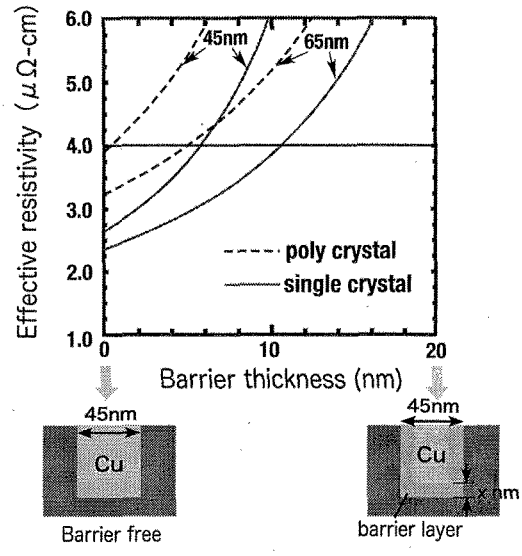

Figure 6 Effective resistivity in Cu damascene interconnects with line width of 65 nm and 45 nm as a function of barrier thickness.

suggested that the grain boundary scattering primarily increased the resistivity of the Cu thin films. We calculated the effective resistivity in nano-scale Cu damascene interconnects and concluded that large grained copper films and ultra-thin barrier layers were essential for low resistance nano-scale Cu interconnects.

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