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Thermal stability and electrical characteristics of ultrathin high-k dielectric metal oxide films on the SiON-passivated Si substrate

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Thermal stability and electrical characteristics of ZrO_2/SiON/Si and $(Zr,Ti)O_2$/SiON/Si gate stacks have been investigated. The layered structures were fabricated by electron-beam deposition of a thin Zr layer and Zr/Ti/Zr multilayer on the SiON-passivated Si substrate, followed by oxidation at 600 ^{0}C in O_2 ambient for 1 hour. The ZrO_2 films are of polycrystalline tetragonal phase. The amorphous Zr-Ti oxide films crystallize as tetragonal or hexagonal ZrO_2 phases after rapid thermal annealing in N_2 ambient above 700 ^{0}C. Both structures were found to be stable with respect to the formation of silicides even after RTA at 1000 ^{0}C. The equivalent oxide thickness of both structures was obtained by capacitance-voltage analyses. The density of interface state of Al/TaN/$(Zr,Ti)O_2$/SiON/p-Si metal-insulator- semiconductor (MIS) structure is higher than Al/TaN/ZrO_2/SiON/p-Si MIS structure due to the ability of Ti to absorb H_2O and O_2.
Key words: high-k, thermal stability, SiON, gate stack

1. Introduction

As SiO_2 is continually scaled down to the sub-1 nm equivalent oxide thickness (EOT) regime, the leakage contribution via direct tunneling becomes excessive and device reliability becomes an issue. Replacement of SiO_2 with a high dielectric constant (high-k) material can significantly reduce gate leakage current with an increased physical thickness while maintaining a low EOT [1]. These dielectrics include Al_2O_3 [2], ZrO_2 [3-6] and HfO_2 [1, 7-9]. Recently, ZrO_2 have been assessed for metal-oxide-semiconductor (MOS) device applications, since it has a high dielectric constant (17-25), a high breakdown field (7-15 MV/cm), and a large band gap (~7.8 eV), and is predicted to be thermodynamically stable on silicon [10].

Previous studies have indicated two major problems when ZrO_2 applying gate process. One is the interfacial oxide growth due to residual oxygen in annealing ambient which causes the increase of EOT [4,11-12]. The other is silicidation due to high temperature annealing (over 900 ^{0}C) under ultrahigh vacuum (UHV) [4-5,12-13]. This silicidation can be ascribed to the desorption of SiO which would be formed by interaction between Si and SiO_2 during high temperature annealing in high vacuum. A small amount of SiO gas can easily change ZrO_2 to $ZrSi_2$ [5]. However, one of the critical requirements for high-k dielectrics is a good thermal stability (up to 1000 ^{0}C, 30 s) of the EOT and leakage current density because of the high temperature process of current complementary MOS (CMOS) fabrication flow. In order to prevent the growth of interfacial oxide and silicidation, a thin passivated layer is required for suppressing oxygen indiffusion and SiO desorption. An ultrathin SiON layer between high-k films and Si substrate was used in the present study.

There is an additional problem when pure ZrO_2 is applied for gate process. Since amorphous ZrO_2 crystallizes at around 500 ^{0}C, the ZrO_2 layers will be crystalline after annealing treatment in conventional CMOS process flow [14]. Crystallization induces grain leakage and nonuniformity in the k value and the film thickness [15]. Previous studies have shown that ZrO_2-Al_2O_3 binary alloys remain amorphous and homogeneous after a rapid thermal process (RTP) anneal at 900 ^{0}C for 1 min. No phase separation has been found in the homogeneous binary alloys before crystallization [14]. Mixing ZrO_2 with Al_2O_3 can strongly increase the crystallization temperature compared to pure ZrO_2, but decrease the dielectric performance since Al_2O_3 has lower k value (k~8-9) than ZrO_2. TiO_2 has a high dielectric constant (k~30) [16], and the ZrO_2-TiO_2 system has been shown to possess good thermal stability. Alloying ZrO_2 and TiO_2 may increase crystallization temperature and maintain the dielectric performance of the high k thin film. In the present study, we focus on the thermal stability of the ZrO_2/SiON/Si and $(Zr,Ti)O_2$/SiON/Si gate stacks, and effects of structural and constituent changes on dielectric performance.

2. Experimental procedures

The substrates used were 8 in., p-type Si(100) wafers with resistivity of 1-10 Ω-cm. A standard cleaning step was employed before gate dielectric growth. Prior to the high k dielectric metal oxide films deposition, a passivated 1.6-nm-thick SiON was grown by N_2 plasma nitridation and O_2 gas annealing. The 3-nm-thick Zr layer and Zr (1.5 nm)/Ti (0.5 nm)/Zr (1.5 nm) multilayer were deposited on the passivated Si substrate by electron beam evaporation at room temperature. The pressure during deposition was 5×10^{-6} torr. The samples were then oxidized under low oxygen pressure (1×10^{-4} torr) at 600 ^{0}C for 1 hour. The samples were divided into two groups: for thermal stability and electrical characteristics measurements.

For thermal stability characteristics, the ZrO_2/SiON/Si and $(Zr,Ti)O_2$/SiON/Si gate stacks were capped by 30-nm-thick amorphous Si films deposited by electron beam evaporation at room temperature. After depositing

the amorphous Si films, heat treatments were carried out in a rapid thermal annealing apparatus at 700-1000 ^{0}C for 30 s in N_2 ambient. Structural characterization was carried out by using a JEOL-4000EX high resolution transmission electron microscope (HRTEM) operating at 400 keV with a point-to-point resolution of 0.18 nm, and a JOEL-2010 transmission electron microscope. The film compositions and chemical bonding states were determined by x-ray photoelectron spectroscopy (XPS). The XPS analyses were done with a PHI 1600 scanning microprobe.

For the electrical measurements, metal-insulator-semiconductor (MIS) capacitors were defined on the gate dielectric stacks. After rapid thermal annealing, a 25-nm-thick TaN film was deposited by sputtering, and a 500-nm-thick Al film was deposited on the gate stacks by a thermal coater. The gate of capacitor was then subsequently defined lithographically and etched. Finally, a 500-nm-thick Al contact was also made to the backside surface of the wafers. High-frequency (100 kHz) capacitance-voltage (C-V) measurements were made on capacitor areas of 1.68 $\times 10^{-4}$ cm^2 using a HP 4284A precision LCR meter connected to a Keithley KI82.

3. Results and discussion

The microstructures of the gate stacks were analyzed by cross-sectional transmission electron microscopy. Figures 1(a)-1(c) show cross-sectional HRTEM images of a-Si/ZrO_2/SiON/Si gate stacks at the as-deposited state and after rapid thermal annealing at 900 and 1000 ^{0}C for 30 sec in N_2 ambient. In Fig. 1(a), well-developed polycrystalline grains were observed in as-deposited gate stack, and the ZrO_2 film exhibits fringes with 0.299 nm spacing that corresponds to the (101) tetragonal ZrO_2 phase. The physical thickness of ZrO_2/SiON gate stack was measured to be about 5.9 nm, which included the passivated SiON film of about 1.5 nm in thickness. In Figs. 1(b) and 1(c), the thickness of SiON film after annealing is almost the same as that of as-deposited film. The adoption of a SiON layer successfully suppresses Si and O diffusion during annealing [17], so that the thickness of interfacial layer did not change markedly after annealing at temperatures up to 1000 ^{0}C.

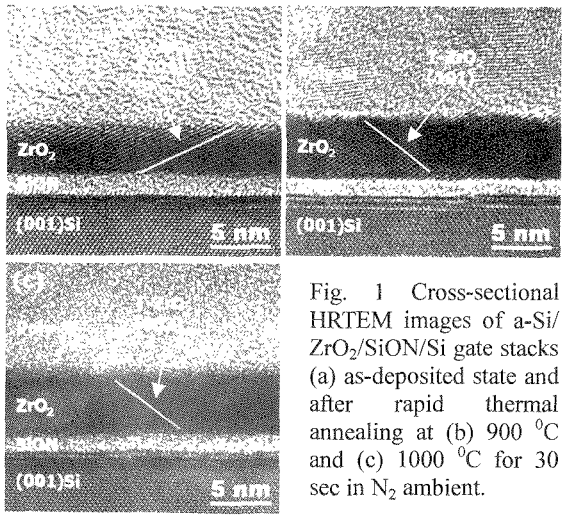

Fig. 1 Cross-sectional HRTEM images of a-Si/ZrO_2/SiON/Si gate stacks (a) as-deposited state and after rapid thermal annealing at (b) 900 ^{0}C and (c) 1000 ^{0}C for 30 sec in N_2 ambient.

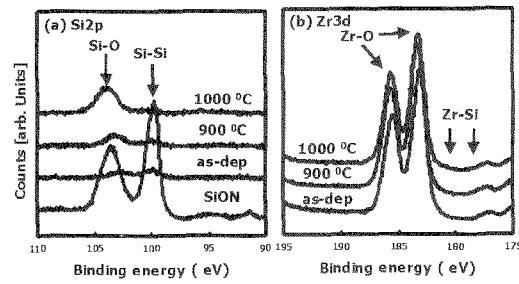

Fig. 2 The XPS analysis (a) before and (b) after rapid thermal annealing of the ZrO_2/SiON/Si gate stack structure showing changes in the Si 2p and Zr 3d spectra. The bottom photoelectron spectra in (a) was obtained form the SiON/Si sample.

From HRTEM image in Fig. 1(c), the interfaces of a-Si/ZrO_2 and ZrO_2/SiON are rather flat, and no interfacial reactions were observed to occur. To analyze a more statistically significant sample area, SAD patterns were obtained with a SAD aperture that included a diffracting area of ~8000 μm^2. Table I shows the phases formed in ultrathin high-k dielectric metal oxide gate stacks on SiON-passivated Si substrate from TEM diffraction pattern (DP) analysis. No Zr-silicide rings were observed in the DP. The SiON passivation makes the a-Si/ZrO_2/SiON/Si gate stacks thermally stable up to 1000 ^{0}C.

The film compositions and chemical bonding states were determined by XPS. Figures 2(a) and 2(b), show changes in Si 2p and Zr 3d core-level photoelectron spectra of the ZrO_2/SiON/Si gate stacks obtained before and after annealing. For the SiON/Si sample, photoelectron peaks of Si-Si bond and Si-O-N bond can be observed. For Zr 3d spectra, it is clear that the Zr atoms are fully oxidized by *ex-situ* reoxidation. After rapid thermal annealing at 1000 ^{0}C for 30 sec, there was no significant change in the photoelectron spectra. The Zr $3d_{5/2,3/2}$ doublet (~178 and 180 eV), which is attributed to the Zr-Si bond, was not observed. The passivated SiON layer successfully suppresses silicidation which is consistent with the DP analysis. It is notable that Zr 3d peak moved toward higher binding energy after annealing. The amount of Zr 3d peak shift is close to that of the chemical shift component of Si 2p spectra. Therefore, the electric charging due to insulating improvement of the gate stacks causes the band bending of interfacial SiON layer for XPS measurement [11, 18].

In order to increase the crystallization temperature of pure ZrO_2 film, the Ti layer is introduced into the Zr layer. From results obtained by DP analyses listed in

Table I. Phases formed in ultrathin high-k dielectric metal oxide gate stacks on SiON-passivated Si substrate identified from TEM diffraction pattern analysis.

	as-deposited	700 °C	900 °C	1000 °C
a-Si/ZrO_2/SiON/p-Si	Tetragonal ZrO_2	Tetragonal ZrO_2	Tetragonal ZrO_2	Tetragonal ZrO_2
a-Si/(Zr,Ti)O_2/SiON/p-Si	Amorphous (Zr,Ti)O_2	Tetragonal ZrO_2	Tetragonal ZrO_2	Tetragonal ZrO_2 + Hexagonal ZrO_2

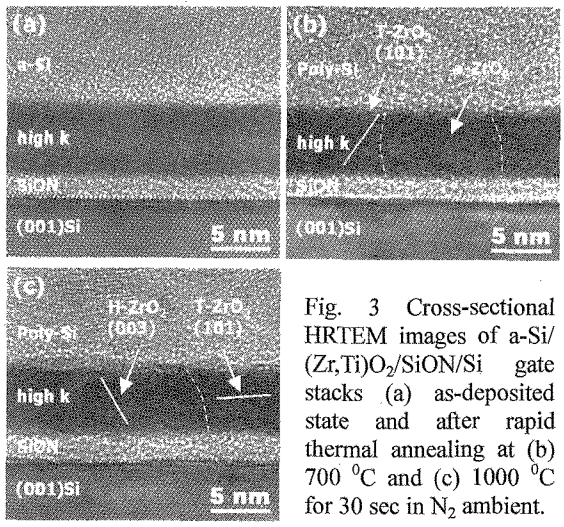

Fig. 3 Cross-sectional HRTEM images of a-Si/ $(Zr,Ti)O_2$/SiON/Si gate stacks (a) as-deposited state and after rapid thermal annealing at (b) 700 ^{0}C and (c) 1000 ^{0}C for 30 sec in N_2 ambient.

Table I, the $(Zr,Ti)O_2$ film is amorphous after oxidation at 600 ^{0}C. After RTA at 700 ^{0}C, the polycrystalline tetragonal ZrO_2 rings began to appear in diffraction pattern. The crystallization temperature of the gate stacks increases to 700 ^{0}C, owing to the mixing of Zr and Ti atoms. Even for annealing up to 1000 ^{0}C, the $ZrSi_2$ phase was not found. Only polycrystalline tetragonal and hexagonal ZrO_2 phases were present. The introduction of Ti atom apparently retarded the formation of $ZrSi_2$ phase, and the a-Si/$(Zr,Ti)O_2$/SiON/Si gate stack is stable at 1000 ^{0}C.

Figures 3(a)-3(c) show cross-sectional HRTEM images of a-Si/$(Zr,Ti)O_2$/SiON/Si gate stacks at the as-deposited state and after rapid thermal annealing at 700 and 1000 ^{0}C for 30 sec in N_2 ambient. In the HRTEM image in Fig. 3(a), it can be seen that the Zr-Ti-O film is of uniform amorphous structure that possesses an atomically flat surface. The two separated layers, Zr and Ti, tend to intermix into a homogenous mixture after oxidation. This implies that homogenous amorphous mixture, $(Zr,Ti)O_2$, is more stable than the two separated layers. The image reveals a 6-nm-thick amorphous $(Zr,Ti)O_2$ film, in addition to the 1.6-nm-thick SiON film. After annealing at 700 ^{0}C, the partially amorphous and crystalline phases were observed as shown in Fig. 3(b). The thickness of polycrystalline tetragonal $(Zr,Ti)O_2$ film was measured to be about 5.7 nm, which was smaller than that of amorphous film. Since the crystalline film become denser.

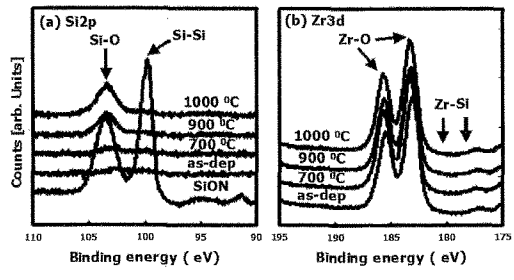

Fig. 4 The XPS analysis (a) before and (b) after rapid thermal annealing of the $(Zr,Ti)O_2$/SiON/Si gate stack structure showing changes in the Si 2p and Zr 3d spectra.

The thickness of the SiON film after annealing is almost the same as that of as-deposited film. With rapid thermal annealing at 800 ^{0}C, the $(Zr,Ti)O_2$ film was found to be fully crystalline. In the HRTEM image in Fig. 3(c), the polycrystalline $(Zr,Ti)O_2$ film shows fringes with 0.299 nm and 0.3 nm spacing that corresponds to the (101) tetragonal ZrO_2 and (003) hexagonal ZrO_2 phase, respectively. No $ZrSi_2$ phase was found in the a-Si/$(Zr,Ti)O_2$/SiON/Si gate stack after annealing at 1000 ^{0}C.

Figures 4(a) and 4(b) show the Si 2p and Zr 3d core-level photoelectron spectra of the $(Zr,Ti)O_2$/SiON/Si gate stacks obtained before and after annealing, respectively. No change was detected in the Si 2p and Zr 3d photoelectron spectra after annealing. For Zr 3d spectra, the Zr-Si bond was not observed, which was the same as that of ZrO_2/SiON/Si gate stacks. The introduction of Ti atom apparently can increase the crystallization temperature to 700 ^{0}C and does not degrade the thermal stability.

For the electrical measurements, MIS capacitors were defined on the gate dielectric stacks. The high frequency C-V curves of the Al/TaN/ZrO_2/SiON/p-Si MIS capacitors with 4.4-nm-thick ZrO_2 and 1.5-nm-thick SiON layer are shown in Fig. 5 for the gate stacks annealed in N_2 for 30 sec for different temperatures. The EOT, which was extracted from the analysis of C-V characteristics, decreases form 3.4 nm (as-deposited) to 2.6 nm after annealing at 900 ^{0}C in N_2. The dielectric constant of ZrO_2 layer can be extracted from the accumulation capacitance using series capacitance model [19]. The largest value of measured capacitance in accumulation is about 223 pF, which corresponds to k ~ 15.6. The dielectric constant of ZrO_2 is almost the same as the value as that reported recently [20-21].

The accumulation capacitance was found to increase with annealing temperatures as shown in Fig. 5. This result may be explained by insulating improvement of the gate stacks after annealing, as obtained from XPS analyses, resulting in the increasing ability to hold charge. One can also see that the C-V curve is stretched out along the voltage axis as the annealing temperature is increased, indicating the increase of the interface state density. Although the samples were annealed in N_2 ambient, there was residual oxygen present in the ambient. The residual oxygen will increase the interface state density during annealing [22].

To check whether the introduction of Ti atom can increase crystallization temperature and maintain the

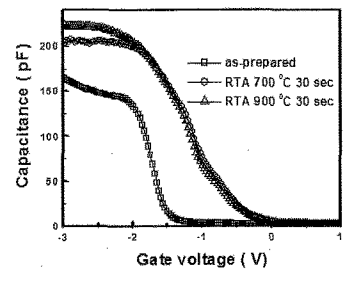

Fig. 5 High frequency (100 kHz) C-V characteristics of the Al/TaN/ZrO_2/SiON/p-Si MIS capacitors after RTA in N_2 ambient for 30 sec at different temperatures.

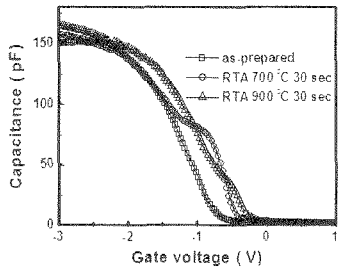

Fig. 6 High frequency (100 kHz) C-V characteristics of the Al/TaN/(Zr,Ti)O_2/SiON/p-Si MIS capacitors after RTA in N_2 ambient for 30 sec at different temperatures.

dielectric performance of the high k thin film, the high frequency C-V curves of the Al/TaN/(Zr,Ti)O_2/SiON/ p-Si MIS capacitors were measured as shown in Figure 6. The accumulation capacitance increases after annealing was observed, owing to the crystallinity of the (Zr,Ti)O_2 film. The amorphous films in as-deposited sample became polycrystalline after annealing.

The EOT of the gate stack and the dielectric constant of (Zr,Ti)O_2 layer has been estimated. The largest value of measured capacitance in accumulation is about 166 pF, which corresponds to k ~ 12.5. The dielectric constant value is smaller than that of the ZrO_2 film. This result shows that the introduction of Ti atom will slightly lower the dielectric performance of the high k thin film.

The stretch-out of the C-V curves was also observed in Fig. 6. Compare Fig. 5 with Fig. 6, it is apparent that the degree of the stretch-out of curves becomes more significant in as-prepared (Zr,Ti)O_2 MIS capacitors than as-prepared ZrO_2 MIS capacitors. It indicates that the density of interface state of (Zr,Ti)O_2 MIS structure is higher than that of ZrO_2 MIS structure. The result may be due to the incorporation of Ti which has an ability to absorb H_2O and O_2. The Ti element can be considered as an additional source of O_2 absorption which increases the interface state density of gate stacks during oxidation.

4. Conclusions

The as-oxidized and annealed in N_2 ambient ZrO_2 films were found to be polycrystalline tetragonal phase. Amorphous thin film of the Zr-Ti oxides after oxidation was observed by HRTEM image and diffraction pattern analysis. The amorphous Zr-Ti oxide films crystallize as tetragonal or hexagonal ZrO_2 phases after annealing above 700 ^{0}C in N_2 ambient. $ZrSi_2$ formation was not observed in both ZrO_2 and Zr-Ti oxides films deposited on SiON-passivated Si substrate after RTA at 1000 ^{0}C for 30 sec. The passivated SiON layer successfully suppresses silicidation.

The electrical characteristics of Al/TaN/ZrO_2/SiON/ p-Si and Al/TaN/(Zr,Ti)O_2/SiON/p-Si MIS structure were investigated. From the analysis of high-frequency capacitance-voltage characteristics, the EOT of the gate stacks and dielectric constant of high k films were obtained. The introduction of Ti atom can increase crystallization temperature and slightly lower the dielectric performance of the high k thin film.

The density of interface states was found to increase after RTA in N_2. The density of interface state of Al/TaN/(Zr,Ti)O_2/SiON/ p-Si MIS structure is higher than that of Al/TaN/ZrO_2/ SiON/p-Si MIS structure due to the incorporation of Ti which has an ability to absorb H_2O and O_2.

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