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Electrical characterization using scanning probe microscopy for microscopic diagnosis of device structure

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Microscopic analysis of device structures based on scanning probe microscopy has been carried out to investigate electrical characteristics such as potential and carrier concentration. A surface-potential distribution was obtained through scanning Maxwell-stress microscopy (SMM). As an in-situ device operation analysis, the surface-potential distribution in a silicon nanowire transistor in operation was measured by SMM. Surface charging observed in the potential image was correlated with the electrical characteristics of the silicon nanowire. As a form of dopant state analysis, the surface potential of silicon implanted with various doping species and concentrations was measured by SMM to correlate the surface Fermi level with the doping conditions. The other important device parameter, carrier concentration, was estimated from the non-linear capacitance obtained by scanning nonlinear dielectric microscopy (SNDM). For quantitative analysis of the carrier distribution at a pn junction in detail, nonlinear capacitance imaging and pin-point capacitance-voltage (C-V) analysis were implemented using SNDM. The results of the pin-point C-V analysis clearly discriminated a depletion layer from tailing of the carrier distribution at the pn junction.
Key words: SMM, SNDM, device operation analysis, doping analysis, Fermi level, pn junction

1. INTRODUCTION

The application of microscopic diagnosis based on scanning probe microscopy (SPM) to electrical characterization of state-of-art integrated circuits has attracted great attention because accurate control of device parameters and an understanding of device operation at the microscopic level have become essential. Electrical characteristics of a device are determined by the distribution of potential and the carrier concentration in the device. Here, we focus our attention on two techniques for microscopic diagnosis - surface potential imaging by scanning Maxwell-stress microscopy (SMM) [1] and non-linear capacitance imaging by scanning nonlinear dielectric microscopy (SNDM) [2]. The surface potential distribution in a device structure reflects the charging of dielectrics [3,4], the work function of materials [5,6] and the semiconductor Fermi level as determined by doping [7]. The nonlinear capacitance - specifically the slope of the capacitance-voltage (C-V) - provides information regarding the conduction type and carrier concentration. We describe our evaluation of surface charges in devices in relation to the electrical characteristics and our doping analysis by means of Fermi level measurement as examples of the diagnostics enabled by SMM. An accurate analysis of carrier concentration at pn junctions is also described as an example of SNDM diagnosis.

2. SURFACE POTENTIAL IMAGING BY SMM

2.1 SMM principle

We applied SPM in air (Seiko Instruments Inc., SPA500) for the SMM measurement. A schematic view of the SMM setup is shown in Fig. 1(a). In the SMM measurement, AC and DC biases were applied between the conductive probe and the sample. The electrostatic force due to the biases caused multifrequency oscillation of the cantilever. The fundamental oscillation component provided the potential image and the second-harmonic oscillation provides the topographic image. The DC bias component V_{DC} was controlled so that the fundamental oscillation component became zero, and thus gave the relative potential of the sample surface to that of the probe (Fig.1(b)). We refer the value of V_{DC} as "SMM potential" in the later discussions. The work function value of the sample surface was derived using the SMM surface potential of Au(111) as the reference material and assuming its work function to be 5.31 eV [8]. The principle of the SMM measurement is described in detail elsewhere [1].

2.2 Device operation analysis

Electrical conduction in a silicon nanowire with an exposed surface is quite sensitive to charges trapped at the wire surface. The charges on the wire surface can be controlled by using a side gate in the vicinity of the wire, and thus the wire exhibits controllability of the threshold voltage V_{th}[4]. Here, we describe our implementation of SMM potential imaging of a silicon nanowire in operation as a clear-cut example of device operation analysis.

We fabricated the silicon nanowires from a p-type (100) silicon-on-insulator (SOI) wafer with 50-nm-thick SOI and 400-nm-thick buried oxide (BOX) layers. The SOI layer was p-type doped ($N_A = 5\times10^{17}$ cm^{-3}). The wire (width W ≈50 nm, length L = 2 μm) and the side

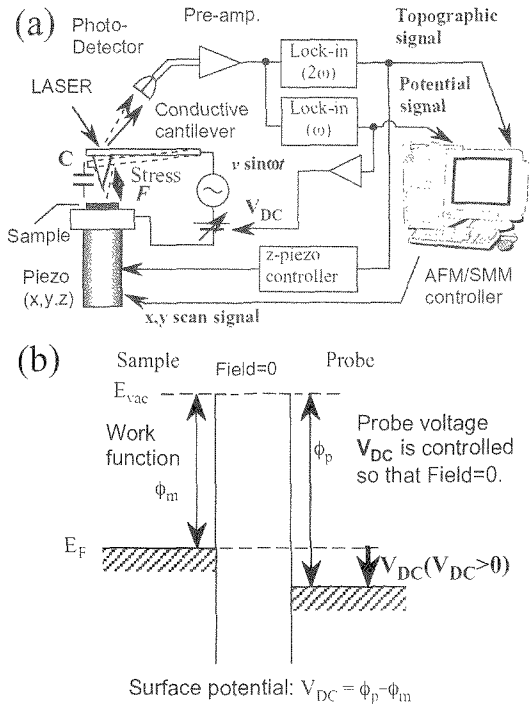

Fig. 1 (a) SMM set up, and (b) principle of work-function measurement by SMM.

gates (gap = 150 nm) were patterned by electron beam lithography using a negative resist (Shipley, SAL601-SR2), and were transferred to the SOI by subsequent reactive ion etching (RIE). Features of the nanowire with the side gates are shown in Fig. 2(a). One terminal of the wire is denoted as the source (S) and the other as the drain (D) in the following discussion. The side gates (SG) were placed parallel to the nanowire. The surface of the nanowire and the side gates were covered with a 5-nm-thick thermal oxide layer. A cross-sectional transmission electron microscopy (TEM) image of the nanowire is shown as an inset in Fig. 2(a).

The SOI substrate was used as the back gate of the n anowire field-effect transistor. The wire current as a function of the back-gate voltage (V_{bg}) was measured as shown in Fig. 2(b). A pulse bias at -30 V was applied to the side gate. The pulse duration was set from 10 ms to 200 ms, and the V_{bg}-I_d characteristics after the pulse voltage application were compared with the initial characteristics. As shown in Fig. 3, the V_{bg}-I_d characteristics of the p-type nanowire shifted toward positive with increased duration of the negative bias to the side gate. The wire conductivity at V_{bg}=0 V increased with increased side-gate bias duration due to the shift of the V_{bg}-I_d curves. The negative pulse bias to the side gate of the p-type nanowire changed the threshold voltage (V_{th}) of the back-gate transistor positively. We consider that the amount of the injected charges on the wire surface increased with the increase in the SG bias duration. The injected charges which remained on the wire for a certain period caused the memorization behavior of the V_{bg}-I_d characteristics.

To confirm the correlation between the surface charging of the nanowire and the conductivity change, we carried out surface potential imaging of the nanowire using by SMM. Figure 4 shows SMM potential images

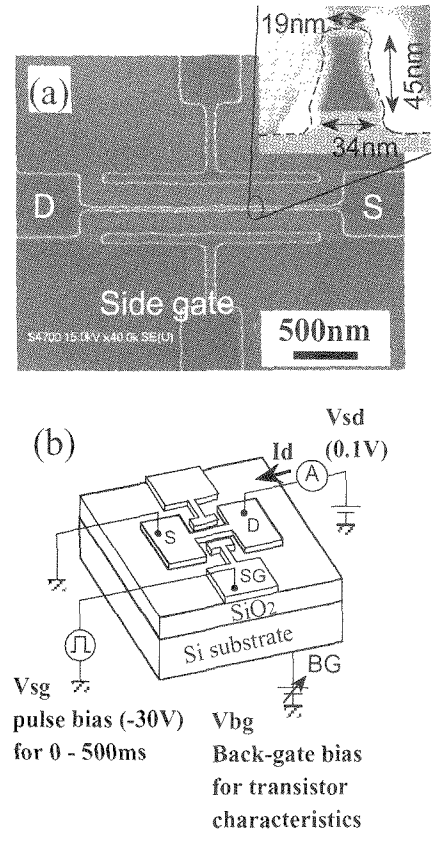

Fig. 2 (a) SEM image of the silicon nanowire with side gates, where the inset shows a cross-sectional TEM image of the nanowire, and (b) schematics of the electrical characterization.

of the p-type silicon nanowire. We varied the side gate voltage (V_{sg}) to reproduce the charging operation during the SMM imaging series. Dotted lines in the image represent the outline of the nanowire and the side gates. The potential images taken at the conductive and non-conductive states were correlated to the sequence of the V_{sg} sweep. After the V_{sg} negative sweep, the contrast in the SMM potential image in the vicinity of the side gates, which included the wire region, turned

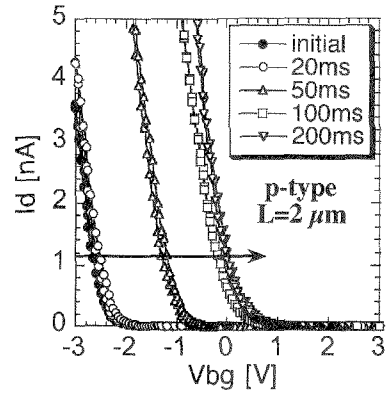

Fig. 3 Transistor characteristics of a p-type silicon nanowire using the SOI substrate as a back gate. Vth was changed by applying a pulse bias to the side gate.

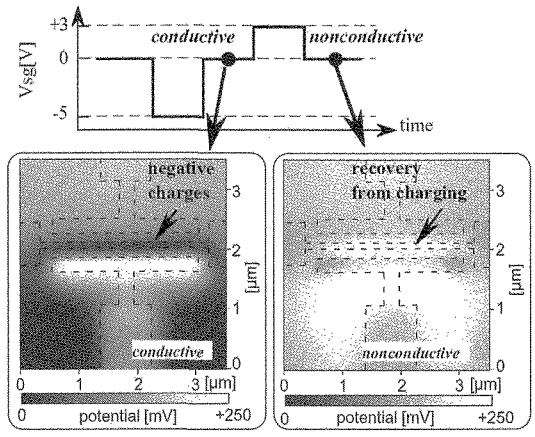

Fig. 4 SMM measurement of the p-type nanowire. SMM potential images after the negative V_{sg} sweep (conductive) and after the positive V_{sg} sweep (non-conductive).

dark; that is, a negative change in the SMM potential occurred at the wire. This condition corresponded to the conductive state of the wire. After the subsequent positive V_{sg} sweep, the dark contrast at the wire disappeared. In other words, the negative charges disappeared from the wire surface. This condition corresponded to the non-conductive state of the wire. Negative charging due to the negative bias applied to the side gate caused hole accumulation in the p-type nanowire which resulted in increased conductivity and the positive V_{th} shift. As mentioned, this evaluation of the charging phenomena through SMM helps us to better understand of the device operation mechanism.

2.3 Doping analysis by Fermi level measurement

We measured the surface potential on silicon wafers having various doping species and concentrations by using SMM to estimate the surface Fermi level. The relationship between the doping concentration and the measured Fermi level was then investigated quantitatively. SMM potential images at a pn junction were obtained and these exhibited profiles that were consistent with the bulk Fermi level determined by doping.

N- and p-type silicon wafers having various doping concentrations were prepared. Boron or phosphorus ions were implanted into Si(100) wafers, and activation annealing was carried out at 1050°C for 60 min. in a N_2 ambient. The estimated doping concentration of each specimen was 7×10^{19} (denoted as n^+) and 1.1×10^{15} cm^{-3} (n) for the phosphorus-doped wafers, and 1.1×10^{19} (p^+), 1.5×10^{16} (p), and 5×10^{13} cm^{-3} (p^-) for the boron-doped wafers. After activation annealing, a 5-nm-thick thermal-oxide layer was grown on the specimens to reduce the influence of Fermi-level pinning by the surface states.

We determined the surface Fermi level of each semiconductor sample E_{fs} by

$$E_{fs}-E_{vac} = V_{probe} - \phi_p, \qquad (1)$$

where E_{vac} is the vacuum level, V_{probe} is the surface potential value given by SMM, and ϕ_p is the work

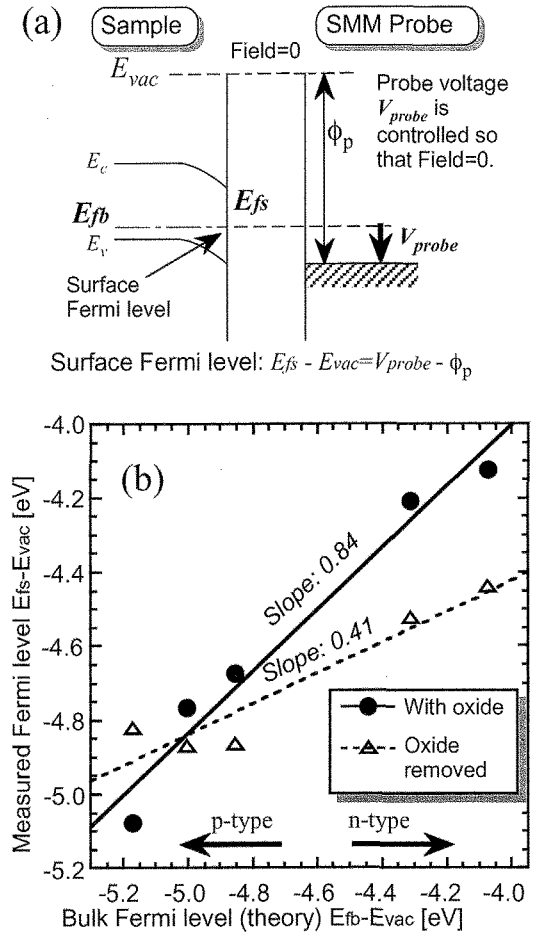

Fig. 5 (a) Definition of the surface Fermi level by measuring the potential through SMM. (b) Relationship between the bulk Fermi level determined by doping and the surface Fermi level measured by SMM.

function of the probe (Fig.5(a)). We converted the average values of the surface potential in the SMM images to the surface Fermi energy using Eq. 1. The estimated surface Fermi energy (E_{fs} - E_{vac}) for the wafers covered with the thermal oxide was 4.126, 4.210, 4.674, 4.769, and 5.076 eV for the n^+, n, p^-, p, and p^+ specimens, respectively. All of these values were between the conduction band E_c - E_{vac} (-4.05 eV) and valence band E_v - E_{vac} (-5.17 eV); that is, within the bandgap of silicon. We calculated the Fermi level in the bulk (E_{fb} - E_{vac}) for each specimen from the doping concentration. The relationship between the bulk Fermi energy and the measured surface Fermi energy is shown in Fig. 5(b). The estimated slope of the relationship for the specimen with the oxide was 0.84, so the surface Fermi energy e stimated by SMM almost coincided with the bulk Fermi energy determined from the doping condition. The measured surface Fermi level for the samples without the thermal oxide, on the other hand, exhibited weaker dependence on the bulk Fermi energy (slope=0.41) than that with the thermal oxide.

The dependence of the surface Fermi level on the bulk Fermi level was influenced by Fermi-level pinning due to the surface states. The Fermi level of the specimens

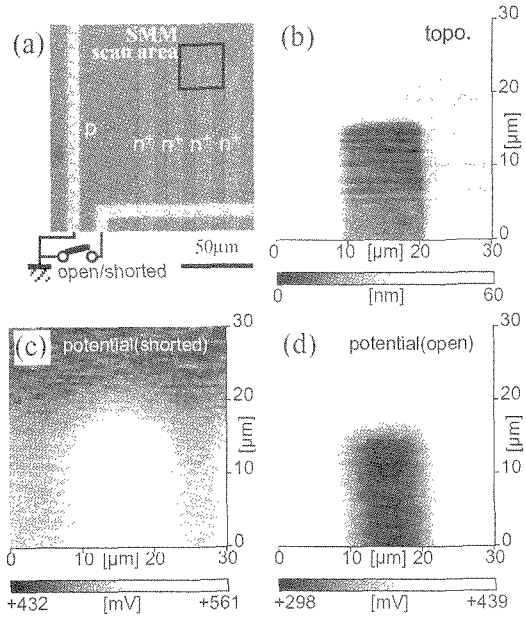

Fig. 6 SMM measurement of the pn junction: (a) Features of the test structure, (b) topographical image, and images of the potential under the (c) short and (d) open circuit conditions.

without the thermal oxide was significantly influenced by Fermi-level pinning due to the high density of the surface states, and thus exhibited weak dependence on the variation in the bulk Fermi level. In the case of interface states at the thermal-oxide/Si(100) interface, on the other hand, the state density was much more suppressed than that without the thermal oxide. Thus, we can suppress Fermi-level pinning caused by the surface states through passivation with thermal oxide; subsequently, quantitative and reproducible estimation of doping becomes possible.

For the purpose of practical doping analysis through SMM, we fabricated test structures of a pn diode. An optical micrograph of the pn-junction test structure is shown in Fig. 6(a). The acceptor concentration of a p-type silicon substrate was set at 5.5×10^{17} cm^{-3} through boron ion implantation. N^+ regions of line-and-space patterns ha ving a width and an interval of 10 μm were formed by arsenic ion implantation (10 keV, 1×10^{15} cm^{-2}). The arsenic was activated by annealing at 950°C for 60 min. The surfaces of the n^+ regions were covered with a 10-nm-thick thermal-oxide layer and the p regions were covered with a 50-nm-thick thermal-oxide layer. Al electrodes were connected to the n^+ and p regions so that the pn junction could be either electrically shorted or in the open condition. We also investigated the influence of the pn junction's electrical connection on the SMM potential images.

The SMM images were taken at the edge of the rectangular n^+ region, as indicated in Fig. 6(a). The n^+ region, which was lower than the surrounding p-region, can be clearly recognized in the topographic image (Fig. 6(b)). The SMM potential image under the electrically shorted condition (Fig. 6(c)) exhibited higher potential in the n^+ region than in the surrounding p region. According to Eq. 1, the higher SMM potential corresponded to a higher surface Fermi level. Thus,

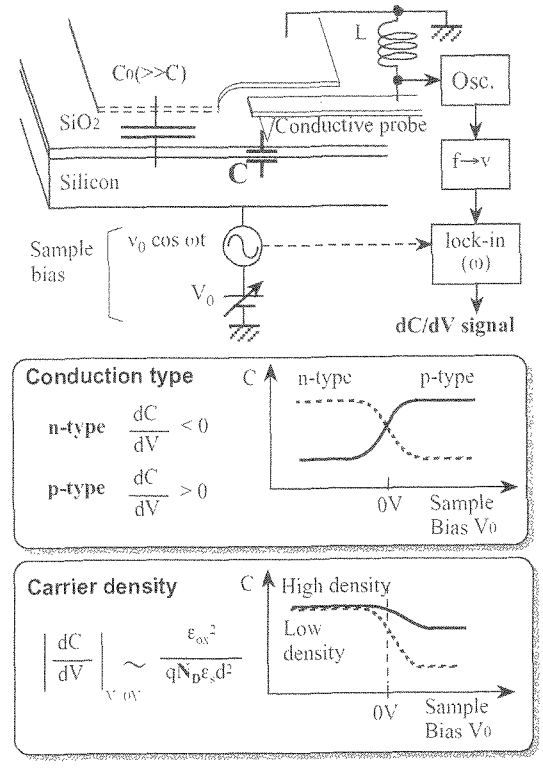

Fig. 7 SNDM setup and analysis of the carrier type and concentration.

the p/n potential contrast in Fig. 6(c) is consistent with the order of the bulk Fermi level. On the other hand, the SMM potential image (Fig. 6(d)) taken under the open-circuit condition exhibited contrast opposite that under the shorted condition - the n^+ region exhibited lower surface potential than the surrounding p region. Surface potential measurement of a pn junction using Kelvin force microscopy (KFM) has been attempted by several researchers [9, 10]. Their results showed higher potential in the n-type region, which is inconsistent with the order of the bulk Fermi level. In their attempts, however, the effect of the electrical connection of the pn junction was not taken into account.

We consider the reason for the inverse potential contrast under the open-circuit condition to be as follows. Generally, a scanning probe microscope uses laser light to detect the probe deflection. We assume that a region on the sample in the vicinity of the probe is irradiated by the laser light. A pn junction under such light irradiation would exhibit a photovoltaic effect. The typical value of the photovoltaic voltage under the open-circuit condition would be about 0.5 V [11]. This photovoltaic voltage, which would change the potential of the n^+ region to negative, would overcome the potential difference due to the difference in the bulk Fermi level (as indicated in Fig. 6(c)) and causes inversion of the p/n potential contrast. In other words, the lower potential in the n^+ region compared to the p region was due to a photovoltaic effects.

3. NONLINEAR CAPACITANCE IMAGEING

3.1 SNDM principle

The principle underlying doping analysis through

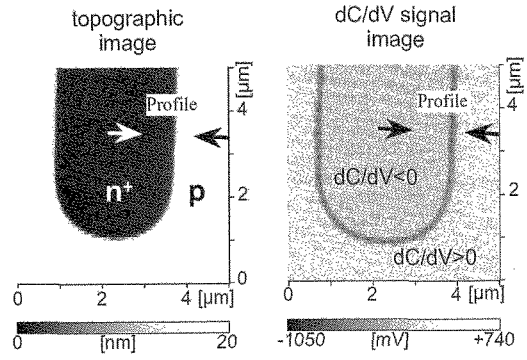

Fig. 8 SNDM measurement of n^+/p junction test structure. Topographic and *dC/dV* signal images for the doping concentration at $N_A=10^{17}$ cm^{-3}.

SNDM is schematically summarized in Fig. 7. SNDM is a variation of a contact AFM. Capacitance (C) between the conductive probe and the sample (SiO_2/Si) is detected from the resonant frequency of the LC circuit. The resonant frequency is influenced in the output voltage of the frequency-voltage converter. AC bias ($v_0 cos\omega t$) is applied to the silicon substrate. The change in C due to the AC bias is influenced in the resonant frequency and extracted by the lock-in amplifier as the *dC/dV* signal. Details of the SNDM principle are described elsewhere [2]. The *dC/dV* signal yields the slope of the C-V curve of the metal-semiconductor-oxide (MOS) structure where the conductive probe plays the role of the metal. As shown in Fig. 7, the slope of the C-V curve (*dC/dV*) for n-type silicon became negative and that for p-type silicon became positive. The amplitude of the *dC/dV* signal was inversely proportional to the carrier concentration (N_D). That is, the sample with a higher doping concentration exhibited a C-V curve with a smaller gradient. We used an SPM unit in vacuum (Seiko Instruments Inc., SPA-300HV) and carried out the SNDM measurements in vacuum (≈1x10^{-5} Pa) with a Rh-coated probe.

3.2 Detailed analysis of a p/n junction

We carried out *dC/dV* signal imaging and C-V analysis by SNDM for the detailed pn junction analysis. The pn diode test structures were fabricated as follows. The doping concentrations of the p-type (Boron-doped) silicon wafers were approximately set at 10^{16}, 10^{17}, and 10^{18} cm^{-3}. N^+ regions were formed by arsenic ion implantation (10 keV, 10^{15} cm^{-2}) and by activation annealing at 950°C for 30 min. The silicon surface was covered with an oxide formed by low-temperature oxidation under ultraviolet irradiation (300°C, 40 min).

Topographic and *dC/dV* signal images of the n^+/p diode ($N_A=1x10^{17}$ cm^{-3}) are shown in Fig. 8. In the topographic image, the arsenic-implanted region, which was lower than the surrounding p-type region, can be clearly recognized. The *dC/dV* image clearly reflects the border of the n+ and the p-type regions. The surrounding p-type region exhibited bright contrast; i.e., $dC/dV > 0$. The border between the n^+ and p-type regions exhibited dark contrast; i.e., $dC/dV < 0$. Moreover, the amplitude of the *dC/dV* signal at the border was greater than that in the n^+ region, suggesting

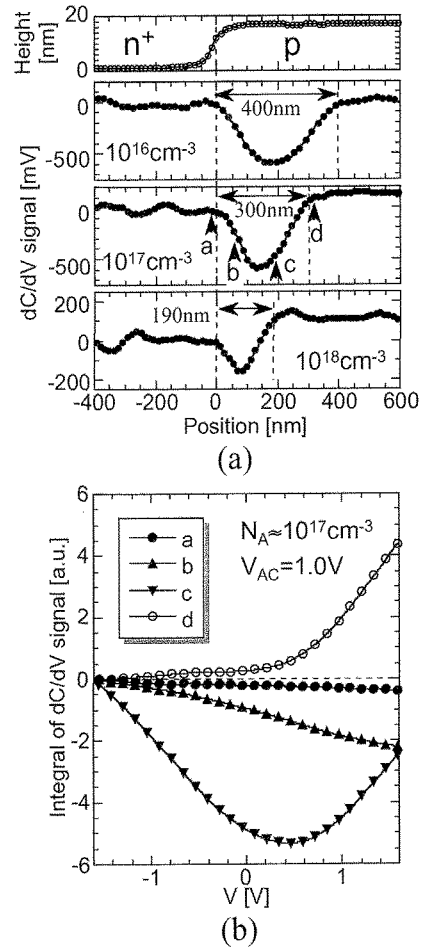

Fig. 9 (a) Profiles of the *dC/dV* signal across the pn junction under different substrate doping conditions. (b) C-V curves measured at four points along the border between n^+ and p-type regions ($N_A=10^{17}$ cm^{-3}).

a lower carrier concentration and the presence of the depletion region.

Profiles of the *dC/dV* signals across the n^+/p junction were extracted from the images and compared for the different substrate doping conditions (Fig. 9(a)). The dip in each profile (i.e., for all doping conditions) corresponded to the dark contrast in the *dC/dV* image. The dip became narrower for the higher doping concentrations. This tendency was consistent with the dependence of the depletion-layer width on the doping concentration.

For a more detailed analysis of the depletion region, we fixed the probe fixed at a certain position and measured the *dC/dV* signals as a function of the DC bias V_0 applied to the sample. The C-V curve was then obtained by integrating the *dC/dV* signal by the voltage. We measured the C-V curves at four points along the dip in the *dC/dV* profile for the doping condition $N_A=10^{17}$ cm^{-3}. As shown in Fig. 9(b), the C-V curve measured at the left edge of the dip (point a) had a slightly negative slope. This C-V curve represents the characteristics of heavily doped n-type silicon. The C-V curve measured at the right-side edge of the dip

(point d) had a positive slope and rose steeply. This C-V curve represents the characteristics of lightly doped p-type silicon. The C-V curve near the n^+ region (point b) had a negative slope and a gradient steeper than that at point a. This C-V cur ve shows that the electron concentration decreased at the point b because of the dopant diffusion in the activation process. The C-V curve taken near the p-type region (point c) had both negative and positive slopes. The bipolar gradient of this C-V curve shows that the probe was within the depletion region and reflects the characteristics of the n- and p-type regions beside the depletion layer.

In a commonly accepted device analysis using scanning capacitance microscopy (SCM), the point where nonlinear capacitance (dC/dV) becomes zero is defined as the junction position from which an effective channel length of a transistor is estimated [12]. The pin-point analysis of the C-V curves obtained by SNDM provides more quantitative information, namely, discrimination of the depletion region from tailing of the carrier concentration due to dopant diffusion.

4. SUMMARY

We have described two microscopic techniques for electrical analysis - surface potential imaging by SMM, and nonlinear capacitance imaging by SNDM. We clarified the correlation between surface charging and controllable V_{th} of a silicon nanowire transistor through in-situ SMM surface-potential imaging. The surface Fermi level of silicon, as an index of the doping state, was measured by SMM. The image of the pn junction potential showed contrast that was consistent with the bulk Fermi level. We carried out a more quantitative analysis of the carrier concentration at the pn junction by SNDM. Non linear capacitance imaging and pin-point C-V analysis at the pn junction enabled us to clearly discriminate the depletion layer and the out-diffusion of carriers.

References

[1] H.Yokoyama and T.Inoue, Thin Solid Films 242, 33-39 (1994)
[2] Y.Cho, S.Kazuta, and K.Matsuura, Appl. Phys. Lett., 75, 2833-2835 (1999)
[3] T.Matsukawa, H.Fujii, M.Nagao, S.Kanemaru, H.Yokoyama, and J.Itoh, Jpn. J. Appl. Phys., 40, 2907-2910 (2001)
[4] T.Matsukawa, S.Kanemaru, M.Masahara, M.Nagao, H.Tanoue, and J.Itoh., J. Vac. Sci. Technol., B21, 664-669 (2003)
[5] T.Matsukawa, S.Kanemaru, M.Nagao, H.Yokoyama, and J.Itoh, J. Vac. Sci.Technol., B19, 1911-1914 (2001)
[6] T.Matsukawa, Y.Murata, T.Kotani, S.Kanemaru, and J.Itoh, Jpn. J. Appl. Phys., 41, 5108-5112 (2002)
[7] T.Matsukawa, S.Kanemaru, M.Masahara, M.Nagao, H.Tanoue, and J.Itoh, Appl. Phys. Lett., 2166-2168 (2003)
[8] H.C. Potter and J.M.Blakely, J. Vac. Sci. Technol. 12, 653-642 (1975)
[9] A.Kikukawa, S.Hosaka, and R.Imura, Appl. Phys. Lett. 66, 3510-3512 (1995)
[10] H.Sugimura, Y.Ishida, K.Hayashi, and O.Takai, Appl. Phys. Lett., 80, 1459-1461 (2002)
[11] S.M.Sze, Physics of Semiconductor Devices, 2nd ed. (Wiley, New York, 1981)
[12] D.M. Tennant, G.L. Timp, L.E.Ocola, M. Green, T. Sorsch, A. Kornblit, F.Klemens, R. Kleiman, Y.Kim, and W.Timp, J. Vac. Sci. Technol. B17, 3158-3163 (1999)

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