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Vertical Double-Gate MOSFET Fabricated Using Ion-Bombardment-Retarded Etching

Meishoku Masahara, Yongxun Liu, Shinichi Hosokawa, Takashi Matsukawa, Kenichi Ishii, Hisao Tanoue, Kunihiro Sakamoto, Toshihiro Sekigawa, Hiromi Yamauchi, Seigo Kanemaru, and Eiichi Suzuki

Nanoelectronics Research Institute,
National Institute of Advanced Industrial Science and Technology (AIST),
1-1-1 Umezono, Tsukuba, Ibaraki 305-8568, Japan
Fax: +81-29-861-3488, e-mail: m.masahara@aist.go.jp

Si wet etching using an alkaline solution was found to be significantly retarded by introducing ion bombardment damage. By utilizing this ion-bombardment-retarded etching (IBRE) phenomenon, a novel process to form an ultrathin vertical channel for a vertical double-gate (DG) MOSFET was successfully developed. Fabricated vertical DG MOSFETs with a 15- to 64-nm-thick vertical channel were shown to exhibit clearly the nature specific to the DG MOSFET, i.e., short-channel-effect immunity by reducing the channel thickness. A novel process for co-integration of vertical DG MOSFETs and planar single-gate (SG) MOSFETs was also demonstrated by applying the IBRE process.

Key words: vertical double-gate MOSFET, ion-bombardment-retarded etching, alkaline solution, ion implantation, wet etching, ultrathin vertical channel

1. INTRODUCTION

In the early 1980s, Sekigawa and Hayashi[1] proved by using simulations that double-gate (DG) MOSFETs provide fundamental advantages such as excellent short-channel effect (SCE) immunity. Since then, DG MOSFETs have been regarded as promising candidates for scalable CMOS devices. Three approaches for the DG MOSFET fabrication are available. The first (planar) involves sandwiching a planar thin channel between top and bottom gates and setting the current to flow horizontally[2]. The second (Fin) involves placing the channel vertically and setting the current to flow horizontally[3,4], similar to the planar fabrication. The last one (vertical) also involves placing the channel vertically, but the current is set to flow vertically to the surface. Among the three types of DG MOSFETs, the vertical one has attracted the most attention due to the scalability of the gate length beyond the lithographic limit and the possibility of high current drivability per unit area[5-7]. It also has the unique strength of usability for a bulk Si substrate instead of a SOI wafer. This is obviously advantageous not only for cutting the process cost but also for suppressing heat accumulation in the active region. Nevertheless, very few studies on vertical DG MOSFETs have been reported[8-10]. This is mainly due to difficulty in fabricating a vertical channel that is thin enough to guarantee a DG MOSFET performance.

Throughout this work, we found that Si wet etching using an alkaline solution is significantly retarded by introducing ion bombardment damage[11]. This phenomenon, named ion-bombardment-retarded etching (IBRE), enables forming an ultrathin vertical channel beyond the lithographic limit. In this work, we fabricated ultrathin vertical channel DG MOSFETs (which we named "IMOSFETs" because of their resemblance to the letter "I") by using the IBRE of Si in hot alkaline solution[12]. In this paper, we briefly describe the IBRE process and its availability for ultrathin vertical channel formation. Then, we experimentally demonstrate the performance of vertical DG MOSFETs with a 15- to 64-nm-thick vertical channel. Finally, we present a novel process for co-integrating a vertical DG MOSFET and a planar single-gate (SG) MOSFET by applying the same IBRE process.

2. VERTICAL CHANNEL FORMATION USING ION-BOMBARDMENT-RETARDED ETCHING

A hot alkaline solution, such as tetramethylammonium hydroxide (TMAH) or hydrazine, is well known to be able to etch the Si substrate anisotropically. The etch rate of Si(111) is significantly lower than other planes. This anisotropical wet etching process has been widely used especially in the field of microelectromechanical system (MEMS) technology[13]. Throughout this work, we found

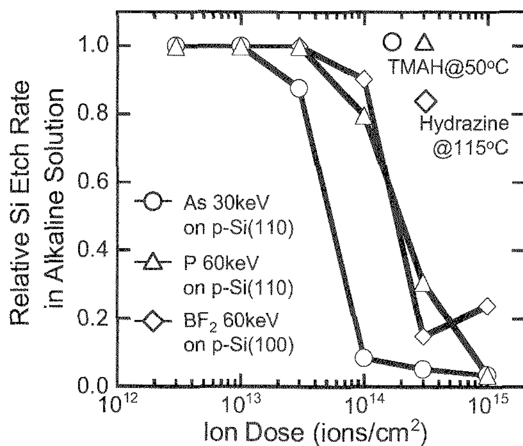

Fig.1 Dependence of relative Si etch rate in hot alkaline solution on ion dose. As ion dose increases, etch rate is significantly retarded, independent of the ion species.

that the Si etch rate (ER) in an alkaline solution is drastically lowered by introducing ion implantation damage independent of the Si surface orientation. Figure 1 shows the relationship between the relative Si ER and the ion dose. The Si ER is markedly decreased as the ion dose increases. It is also obvious from Fig. 1 that the IBRE can occur independent of ion species, surface orientation, and species of an alkaline solution. This phenomenon arises from the suppression of an electrochemical reaction between the Si substrate and alkaline solution due to the increased resistivity of as-implanted Si. It is apparent from Fig. 1 that a dose of 1×10^{15} cm^{-2} is enough to make an etching mask layer for an alkaline solution. Our ultrathin vertical channel is fabricated using the following three steps shown in Fig. 2. First, a SiO_2 mask with a line pattern is formed in parallel with the <112> direction. Then, a sample is dipped in hot alkaline solution to form a thicker vertical channel (Fig. 2(a)). Because the Si (111) plane has an extremely low ER compared with other planes, (111)-oriented side walls that are perfectly vertical to the surface can be fabricated. Next, keV ions are implanted on the vertical channel perpendicularly (Fig. 2(b)). As a result, ion implantation damage appears at the top and bottom of the channel, while the side walls remain unexposed. Finally, the sample is dipped again in the hot alkaline solution, where the top and bottom damaged regions act as etch stoppers due to the IBRE, and unexposed sidewalls are etched horizontally (Fig. 2(c)). The ER of a (111)-oriented Si sidewall is low enough to ensure high control of the vertical channel thinning. A cross-sectional SEM picture of the vertical channel after the IBRE is shown in Fig. 2(d). Figure 2(d) clearly indicates that the region exposed by the ion beam serves as an etch mask, and the 15-nm-thick vertical channel is successfully formed. If we use the dopant ions for the IBRE, the ion-exposed regions, i.e., the top and bottom of the channel, turn into the drain and source automatically.

3. DEVICE FABRICATION

The process flow of the IMOSFET is very simple. We used p-type Si (110) wafers with 15 Ωcm resistivity. A vertical channel of 150 nm in height and 24 μm in length was formed in an isolated active region. Both the wet etching for a thicker vertical channel formation using an SiO_2 mask and the thinning of the channel using the IBRE were performed in 2.38% TMAH at 50°C. For the IBRE and source/drain formation, 30 keV As ions with a dose of 1×10^{15} cm^{-2} were perpendicularly implanted to the Si substrate with thicker vertical channels. The dopant activation was performed during the gate oxide (7 nm) formation using pyrogenic technique. Conservatively thick gate oxide is not inherent in the IMOSFET structure. This thickness was chosen to provide a satisfactorily thick oxide on the channel top for masking the channel during

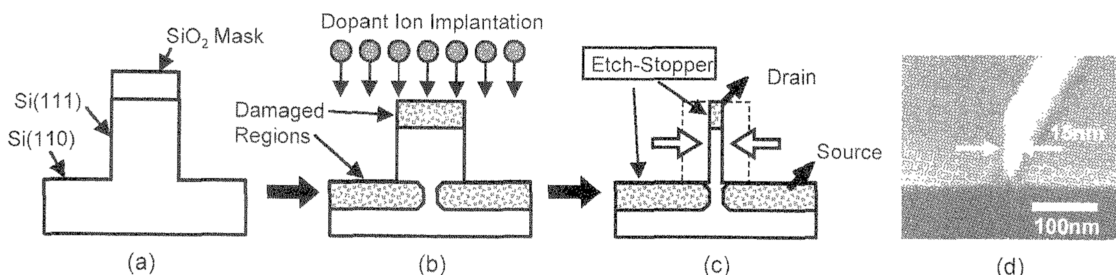

Fig. 2 Ultrathin vertical channel formation by utilizing IBRE: (a) thick vertical channel formation by vertical etching using SiO_2 mask, (b) mask SiO_2 stripping and ion implantation, (c) ultrathin vertical formation by using IBRE, and (d) SEM image of fabricated ultrathin vertical channel.

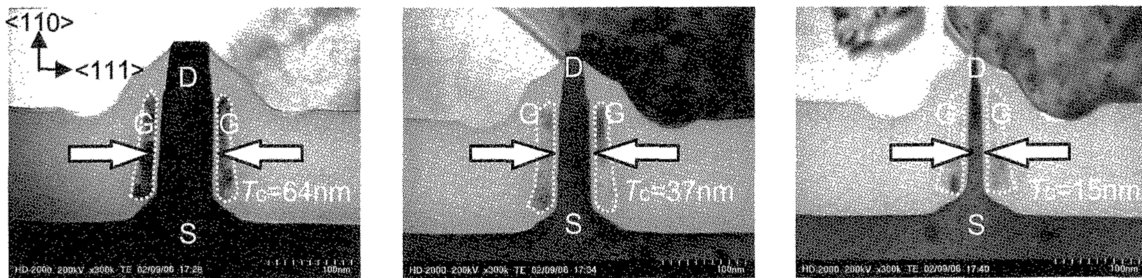

Fig. 3 Cross sectional STEM images of fabricated IMOSFETs with channel thickness of 15- to 64-nm Thicker oxide between the source and the gate results from an enhanced oxidation rate due to amorphization by ion implantation and a higher oxidation rate in the Si (110) plane.

the polysilicon overetch. After the oxidation, in situ P-doped poly-Si was deposited conformally on the channels. To form a symmetrical side DG on both sides of the vertical channel, we adopted a self-aligned etchback process that is commonly used for sidewall spacer formation in fabricating lightly-doped drain (LDD) MOSFETs[14]. An anisotropical RIE with SF_6/O_2 mixture was used to remove the polysilicon leaving the side gates abutting on each side of the channel. The gas pressure and etching power were optimized to prevent polysilicon surface damage caused by the etching. The poly-Si gate was overetched from the top of the channel to facilitate oversized drain contacts. We adopted the planarization and etchback process[15] using the electron beam (EB) resist to open the contact hole self-aligned to the vertical channel. The metallization completed the IMOSFET fabrication after the drain contact formation. The total thermal budget was within 10 min at 850°C. Because the drain and source can be formed prior to the gate oxide growth, the developed process enables high-k materials to be incorporated into the gate insulator and metals into the gate electrode, both of which require a low temperature process. The gate and channel length are 120 nm and 24 μm, respectively.

4. DEVICE RESULTS

Cross-sectional STEM images of fabricated IMOSFETs with a 15- to 64-nm-thick vertical channel are shown in Fig. 3. Note that the channel surface orientation and the current direction are <111> and <110>, respectively. The channel thickness for the thinnest IMOSFET was found to be 15 nm. To our knowledge, this is the thinnest channel vertical DG MOSFET reported. It is noteworthy that the thickness of the oxide grown between the source and the gate is considerably thicker than the gate oxide. This originates in an enhanced oxidation rate caused by amorphization because of implantation and a higher etch rate of the Si (110) surface than that of the Si (111). This is desirable to reduce the overlap capacitance between the gate and the source. Because no channel doping was performed and dopant ions were implanted perpendicularly to the channel, the dopant concentration in the channel was estimated to be an n-type of 10^{17} cm^{-3} by a process simulation[16]. It is apparent from Fig. 4 that the subthreshold characteristics of the fabricated IMOSFETs were improved while decreasing the channel thickness, T_c, even for a thick gate oxide of 7 nm. This improvement precisely demonstrates the unique nature of a DG MOSFET structure. In addition, extremely low gate induced drain leakage (GIDL) current is observed in the I_d-V_g curve for the thinnest vertical channel IMOSFET. Choi et al. suggested that the GIDL is essentially suppressed by a DG structure and that it decreases as the channel thickness decreases[17]. These results

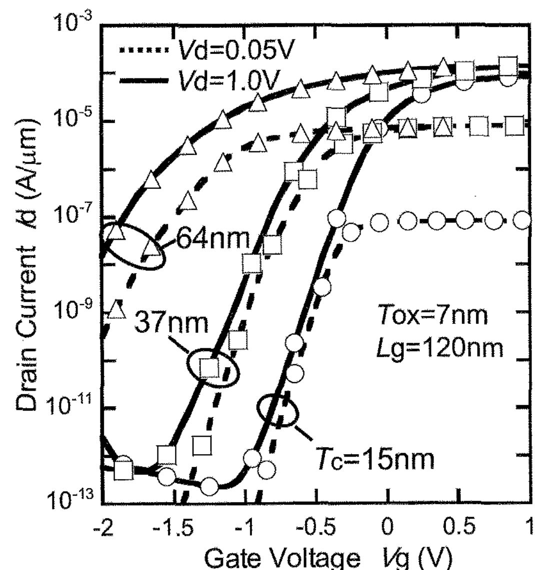

Fig.4 Measured subthreshold I_d-V_g characteristics of fabricated IMOSFETs with 15- to 64-nm-thick vertical channel. As the channel thickness is thinned down to 15 nm, SCEs are totally suppressed even for a relatively thick gate oxide of 7 nm.

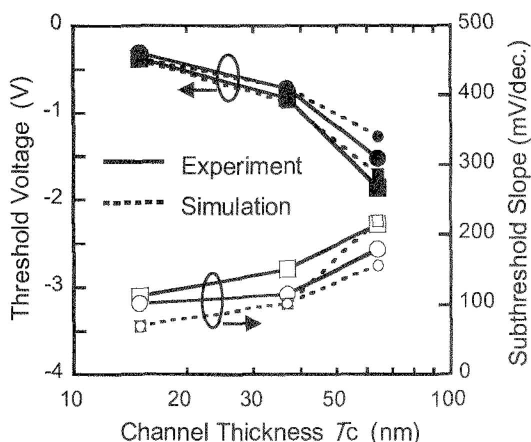

Fig.5 Dependencies of V_{th} and S-slope on channel thickness. Circles and squares indicate saturation mode and linear mode, respectively. Experimental data (solid line) is in good agreement with the data obtained via simulation (broken line).

were explained by the reduction in the transverse electric field at the drain surface and the increase in the transverse effective mass as the channel thickness decreased. The unsatisfactory on-current mainly arises from the thick gate oxide and the series resistance of the source and drain region. We intend to reduce the parasitic resistance of the source and the drain contact resistance by both salicidation of the source and enlargement of the drain by further improving the IBRE process. Device parameters obtained experimentally are plotted in Fig. 5 as a function of the T_c. As one can see in Fig. 5, the SCEs, such as increases in drain induced barrier lowering (DIBL) and subthreshold slopes (S-slope), are totally suppressed as the T_c decreases. The experimental data is compared with that estimated using the process and device simulation[18] as also shown in Fig. 5. The experimental data is in good agreement with the simulated results. In the simulation, the conventional drift-diffusion model was used. Therefore, it seems reasonable from the observed agreement to suppose that quantum mechanical effects are not significant until T_c = 15 nm.

By utilizing the same IBRE process, we have succeeded in fabricating p-ch IMOSFETs. For the p-ch IMOSFET case, BF_2 ions were used for the IBRE process. The details are described elsewhere[19].

5. CO-INTEGRATION OF DOUBLE-GATE AND SINGLE-GATE MOSFET

Vertical DG MOSFETs have a significant drawback in that the designer has few choices for the gate length on a given chip. One possible solution to this problem is co-integrating vertical DG MOSFETs and standard planar SG MOSFETs on a single chip[20]. Thus, we have developed a simple process for the co-integration to maximize the circuit design simplicity and circuit performance[21]. The co-integration of vertical DG MOSFETs and planar SG MOSFETs was achieved by augmenting the conventional CMOS process with the IBRE of Si in a TMAH solution. No difference exists between the vertical DG and

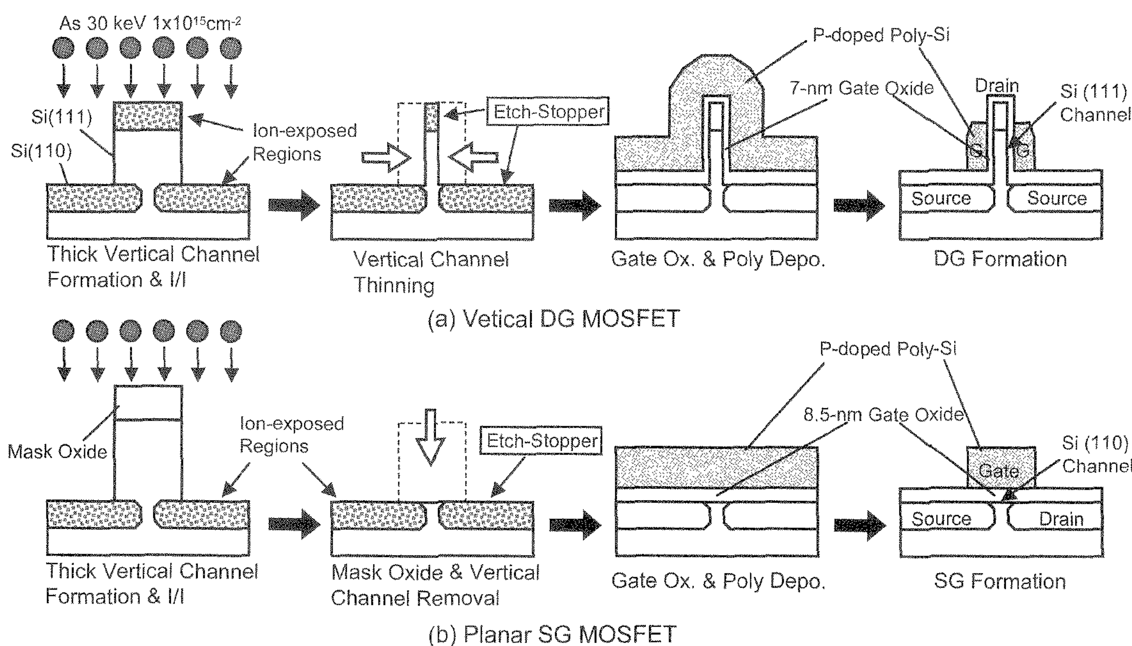

Fig. 6 Comparison between (a) vertical DG MOSFET fabrication process flow and (b) planar SG MOSFET one. The difference in the gate oxide thickness between DG and SG originates in a higher oxidation rate of the Si (110) plane than that of the Si (111) plane.

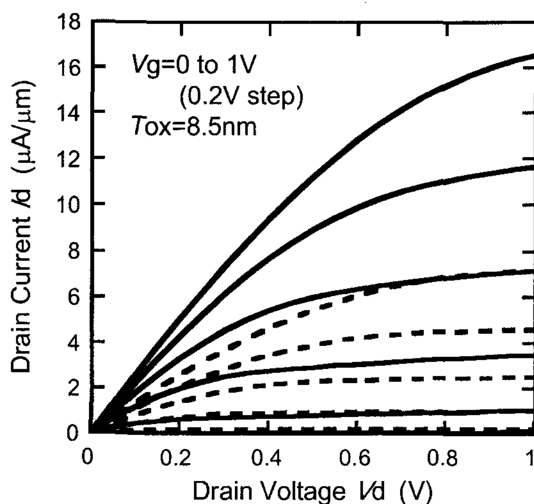

Fig.7 Measured I_d-V_d characteristics of the planar SG MOSFETs with L_g= 2μm (solid lines) and L_g= 5μm (dashed lines). The on-current is enhanced as the gate length shrinks.

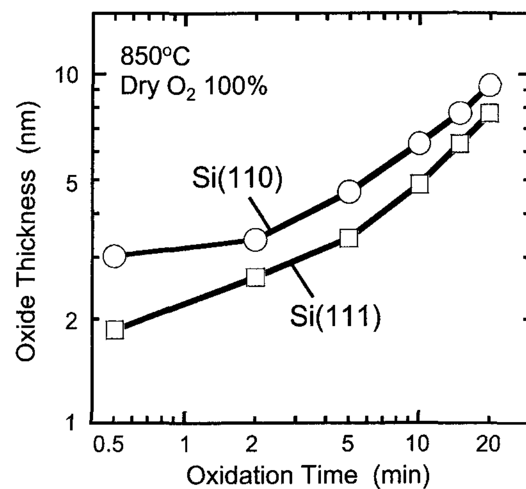

Fig.8 Comparison of oxidation rates between (110) plane and (111) plane. The oxidation rate of the (110) plane is always higher than that of the (111) plane for oxide below 10 nm.

planar SG MOSFET processes, other than in the step order of the mask SiO_2 stripping process, as shown in Fig. 6. In either case, we first form a thicker vertical channel. After that, in the vertical DG case (Fig. 6(a)), the mask SiO_2 is completely stripped. Then, dopant ions are perpendicularly implanted onto the channel, and the channel is thinned by using the IBRE process. However, in the planar SG case (Fig. 6(b)), the mask SiO_2 is removed after the ion implantation, so that ion implantation damage does not occur at the top of the channel. After stripping the SiO_2 mask, the sample is dipped in a hot TMAH, where a planar channel appears. Finally, the gate oxidation and gate electrode formation are performed for vertical and planar channels. Figure 7 shows that the planar SG MOSFET fabricated using this process works normally. As the gate length shrinks, the on-current is enhanced. Note that the channel is an Si (110) plane for the planer SG-MOSFET, while Si (111) is for the vertical DG MOSFET. Figure 8 shows the growth rates of oxides for Si (111) and Si (110) planes. It is apparent that the oxide grown on the Si (110) plane is thicker than that on the Si (111) plane. Thus, the described process enables automatically co-integrating planar SG MOSFETs with thicker gate oxides and DG MOSFETs with thinner gate oxide. This is very advantageous for a system-on-a-chip (SOC), in which multiple gate oxide thicknesses are strongly required on the same substrate for low power consumption.

6. SUMMARY

We fabricated vertical DG MOSFETs ("IMOSFETs") with a 15- to 64-nm-thick vertical channel on a bulk Si substrate using the discovered IBRE phenomenon. The thinnest channel IMOSFET shows the unique nature of the double gate MOSFET structure. A novel process for co-integration of a vertical DG MOSFET and a planar SG MOSFET was successfully developed by utilizing the IBRE phenomenon.

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