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The Nano-CMOS era. Will CMOS be scaled beyond the roadmap?

(Invited talk)

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Abstract
Historically, innovations have been possible because of the strong association of devices and materials research. The demand for low voltage, low power and high performance are the great challenges for engineering of sub 50nm gate length CMOS devices. We point out the main issues to address in order to investigate and push the limits of CMOS technology. The alternative architectures allowing to increase devices drivability and reduce power are reviewed. Among the materials options to be integrated, HiK gate dielectric and metal gate are among the most strategic options to consider for power consumption and low supply voltage management. New architectures and options are reviewed through the issues to address in gate/channel and substrate, gate dielectric as well as source and drain engineering. It will be very difficult to compete with CMOS logic because of the low series resistance required to obtain high performance. By introducing new materials, Si based CMOS will be scaled beyond the ITRS as the future System-on-Chip Platform integrating new disruptive devices. Functionality of devices in the range of 5 nm channel length has been demonstrated showing that CMOS technology could still be used in the future if we manage to implement new materials and device architecture options.

Key words: CMOS, Nano, roadmap, HiK, Metal gate, Nanocrystals, Flash memory.

1. INTERNATIONAL TECHNOLOGY ROADMAP OF SEMICONDUCTORS ACCELERATION AND ISSUES.

Since 1994, the International Technology Roadmap for Semiconductor (ITRS)[1] (Figure 1) has been accelerating the scaling of CMOS devices to lower dimensions continuously despite the difficulties that appear in device optimization. However, uncertainties about lithography, economics and physical limitations can probably slow down the evolution. For the first time, since the introduction of poly gate in CMOS devices process, showstoppers other than lithography appear to be deserved special attention and could require some breakthrough or evolution if we want to continue scaling at the same rate. Design could also be affected by this evolution.

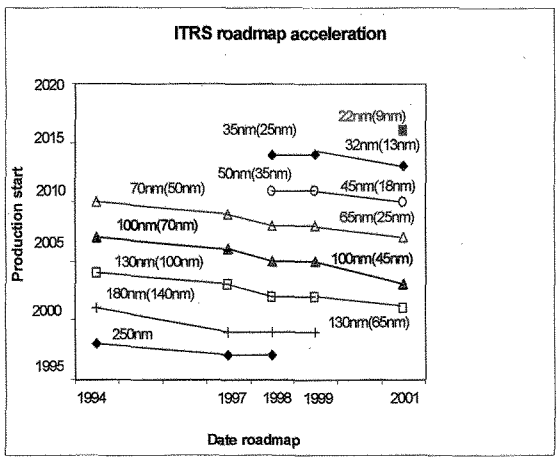

Figure 1 ITRS roadmap acceleration since 1994[1]. Example for MPU and ASICs

Which are the main showstoppers for CMOS scaling? In this chapter, we focus on the possible solutions and guidelines for research in the next years in order to propose solutions to enhance CMOS performances before we need to skip to alternative devices. In other words, how can we offer a second life to CMOS ?

To that respect, the roadmap distinguishes today three types of products: High Performance(HP), Low Operating Power(LOP) and Low Standby Power(LSTP) devices. In the HP case, a historical fact will happen by the 32nm node: the contribution of static power dissipation will become higher than dynamic power contribution! In this papaer we will analyze the various mechanisms giving rise to leakage current in a MOS device and can impact consumption of final devices. Gate leakage current is already a concern. In the case of LSTP devices, a HiK gate insulator could be needed earlier than expected in order to limit static consumption(see section 4.2).

2. LIMITATIONS AND SHOW STOPPERS COMING FROM CLASSICAL CMOS SCALING.

Several mechanisms can generate devices leakage in ultra small MOSFETs. which can be sorted in two categories:

a)Classical type.

- Drain Induced Barrier Lowering(DIBL) is due to the capacitive coupling between source and drain.

• Short Channel Effect(SCE) due to the charge sharing in the channel in the short channel devices at low Vds.
• Punch-Through between source and drain due to the extension of source space charge to the drain.
b) Quantum and high field effects
• Direct tunneling through the gate dielectric.
• Field assisted tunneling at the drain to channel edge. This effect occurs if electric field is high and tunneling is enhanced through the thinnest part of the barrier.
• Direct tunneling from source to drain. This effect will occur in silicon for a thicker barrier than on SiO2 because the barrier height is lower and the equivalent barrier thickness is higher, due to the higher dielectric constant.

Velocity overshoot and ballistic transport are the mechanisms that will enhance drivability in sub 100nm channel lengths devices. However, the impact of scattering by dopants on transport is not negligible even in 5nm range channel lengths [2][3]. Superhalo is efficient to improve SCE and DIBL in 16nm finished gate length(Figure 2)[4] This effect is balanced by the dopant diffusion effect on the channel transport properties degradation.

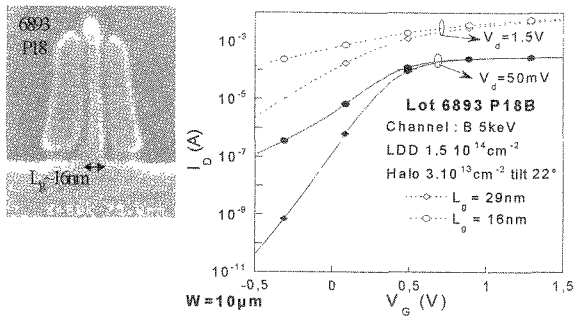

Figure 2 Functional Finished gate length 16nm MOSFET sub threshold characteristics. Gate oxide thickness is 1.2nm[3]. Isat is 600µA/µm.

3. ISSUES IN LOWERING SUPPLY VOLTAGE.

In the future, the electronics market will request portable objects used in daily life and thus low standby and active power dissipation. For sub 0.10µm devices, the following main issues cannot be avoided:

3.1) Direct tunneling through SiO2 is significant for a thickness less than 2.5 nm. It contributes to the leakage component of power consumption. 1.4 nm thin SiO2 is usable without affecting devices reliability[5][6],[7],[2].

3.2)High doping levels in the channel reaching more than $5x10^{18}$ cm^{-3} enhances Fowler-Nordheim field assisted tunneling reverse current in sources and drains up to values of 1A/cm2 (under 1V)[8].

3.3)Classical small dimension effects are more severe than the fundamental limits of switching (quantum fluctuations, energy equipartition, or thermal fluctuations). A minimum value is required for threshold voltage due to:
* *subthreshold inversion.* For ideal fully-depleted SOI(FDSOI) 59.87 mV/dec subthereshold swing can be obtained at 300K. The limit VT value is 180mV precluding a supply voltage V_S lower than 0.50V. Impact Ionization MOS (I-MOS) would allow to reduce subthreshold swing to 5mV/dec. However, performance remains an issue[9].

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* *short channel effect* due to the charge sharing along the transistor channel following the relation:

$$\Delta V_T = -4\varphi_F \frac{C_w}{C_{ox}} \frac{x_j}{L}\left[\left(1+2\frac{W}{x_j}\right)^{1/2}-1\right] = -4\varphi_F \frac{\varepsilon}{\varepsilon_{ox}} \frac{t_{ox}}{L} \frac{x_j}{W}\left[\left(1+2\frac{W}{x_j}\right)^{1/2}-1\right] \quad (1)$$

Here VT is expressed by: $V_T = V_{FB} + 2\varphi_F - \frac{Q_B}{C_{ox}}$ (2)

where $V_{FB} = \varphi_{MS} - \frac{Q_{ox}}{C_{ox}}$ (3) and $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$;

$\varphi_{MS} = \varphi_M - \varphi_s$ (3.1)

ΔV_T is the threshold voltage decay; t_{ox} is the gate dielectric thickness; $\acute{\varepsilon}$ and $\acute{\varepsilon}_{ox}$ are the silicon and gate dielectric constant respectively; L is the channel length; X_j is the drain or source junction depth; W is the space charge region depth; V_T is the threshold voltage ; V_{FB} the flatband voltage ; ϕ_F the distance from Fermi level to the intrinsic Fermi level ; Q_B the gate controlled charge ; C_{ox} is the unit area capacitance of the gate insulator. φ_{ms} is the difference between the extraction potentials of the gate and the semiconductor; Q_{ox} is the oxide charge density ; φ_M and φ_S are the metal and the semiconductor workfunction.
Gate depletion and quantum confinement in the inversion layer will play an important role on short channel effect by adding their contribution to the gate to channel capacitance C_G. SCE is the main limitation to minimal design rule. For low VT values it can be of the order of VT. In order to maintain inverter delay degradation to less than 30% , we must observe the condition $V_T = \frac{V_S}{3}$ [10].

3.4) Statistical dopant fluctuations. The effect of dopant fluctuations has already been considered by Schockley in 1961[11]. Recently, special attention is being paid to this subject because the number of dopants in the channel of a MOSFET tends to decrease with scaling[12], [13]. The random placement of dopants in the MOSFETs channel by ion implantation will affect devices characteristics for geometries lower than 50 nm. The discrete nature of dopant distribution can give

rise to devices characteristics asymmetry[13].

Dopant fluctuations and Fowler Nordheim limitation at high electric field will encourage the use of low doped thin SOI.

4. MOSFET OPTIMIZATION

Possible solutions to overcome the physical limitations encountered in classical scaling are reviewed through:

- gate stack and channel/substrate engineering
- source and drain engineering
- gate dielectric engineering

4.1. Gate stack and channel /substrate engineering.

4.1.1. Gate and channel. Issues in classical scaling of bulk MOSFET

Gate and channel engineering must be optimized together because both physical characteristics affect the nominal VT value of expression (2) which can be written as :

$$V_T = V_{FB} + 2\Phi_F - \frac{Q_B}{C_G} \quad (4)$$

(gate depletion and channel quantum effects are taken into account).

Low VT values will result from:

4.1.1) adjusting gate insulator thickness(see section 4.2).

4.1.2) tuning surface doping concentration as low as possible. Excellent localization of the dopant profile is needed to minimize junction parasitic capacitance and body effect. Selective Si epitaxy of the channel has also been suggested to achieve almost ideal retrograde profiles[14].

4.1.3) Strained channel engineering

Strained SiGe[15], SiGexCy based alloys or strained Si epitaxy have been studied to increase the channel mobility [16][17]. However, high quality gate insulator and subthreshold characteristics optimization require a Si cap layer on top of the channel and low thermal budget[17]. HiK gate insulator is needed in these architectures[18]. Selective epitaxial Si:C acts as Boron diffusion barrier (Figure 3) and thus help to improve drastically short channel effect[17] as well as low field mobility.

4.1.4) choosing the gate material.

Ideal transfer CMOS inverters characteristics requires symmetry of threshold voltage for n and p channel devices (i.e.VTP=-VTN). Several alternatives have been envisaged :

- *the use of n+ poly gate for nMOSFET and p+ poly gate for pMOSFET.* This solution suffers from Boron penetration into SiO2 coming from the p+ doped gate. Nitrided SiO2 *limits without avoiding* this effect: trapping centers are created near or at the SiO2/Si interface decreasing carrier mobility.
- *the use of metal gate material.* No gate depletion is observed in this case. The use of midgap gate(TiN for example)on bulk or partially depleted SOI will be dedicated to supply voltages higher than 1V. Workfunction engineering for Dual metal gates, is challenging: the highest CMOS performance/lowest leakage current trade off can be obtained. It is mandatory on low doped FDSOI.

Several approaches have been proposed for metal gate integration. The classical process integration requires the protection of the metal gate material from ion implant as well as oxidation during the dopant activation anneal. TiN is often chosen as a gate material[19], because it is available as a standard in the industry. Integration with Ta2O5[20,21]has been reported : however leakage current is an important issue. Alternatives such as the damascene gate (Figure 4)[22,23] have been achieved in order to avoid the source

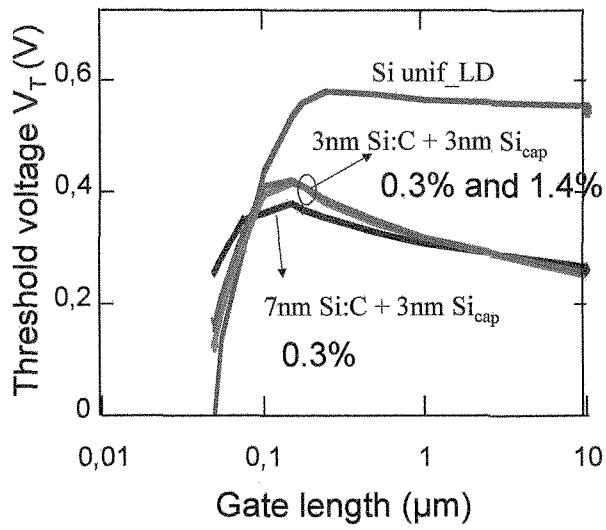

Figure 3 Effect of introduction of Carbonated silicon in MOSFET channel on Short Channel effect.[17]

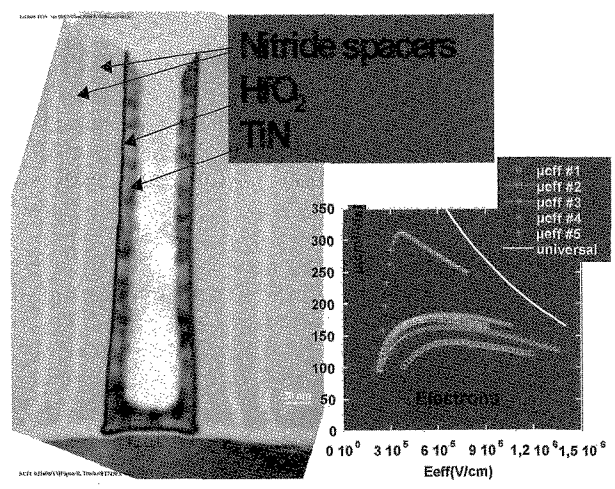

Figure 4 TEM cross section of TiN/HfO2Damascene gate stack[23]. Electron Mobility degradation with HiK inserted.

and drain activation temperature issue. High Frequency and Multi threshold devices could be embedded in Systems On Chip thanks to the damascene architecture.

4.2) Gate dielectric engincering.

The gate leakage due to direct tunneling in standard SiO2 or SiOxNy is one major show stoppers[1]. It will impact directly the static power dissipation Pstat according to the relation :

$P = P_{stat} + P_{dyn}$ (5) $P_{stat} = V_{dd} x I_{off}$ and $P_{dyn} = C V_{dd}^2 f$ (6)

P being the total power dissipation; P_{stat} being the static power dissipation; P_{dyn} being the dynamic power dissipation. If one considers a circuit with active area of the order of 1cm2 and gate oxide tox=1.2nm . If Ioff is due to gate leakage, then considering Vdd=0.5V then Pstat(0.5V)= 5W. We would get Pstat(1.5V) = 750W for a Vdd of 1.5V!! This is a major show stopper for scaling of CMOS technology. That is why High K will be needed in the near future. Besides affecting static power, gate leakage impacts also negatively delay time [24]and affects the functionality of logic circuits.

A decrease of devices performance has been reported if SiO2 thickness is lower than 1.3nm[25] suggesting a surface roughness limited mobility process due to the proximity of sub-oxide. The strong band bending due to quantum mechanical corrections affects the lower limit of supply voltage in the constant field scaling approach[26]. Solutions compatible with silicon gate are also investigated to keep compatibility with a standard CMOS process flow: HfSiOx, ZrSiOx are given much attention as good candidates[27]. These solutions are *dielectric thickness budget* consuming(SiOx interface) and Fermi level pinning occurs at the HiK/poly gate interface[28].

Recently, the lowest leakage current has been reported by using 1.3nm EOT HfO2 combined with a TiN gate integrated on 45 nm CMOS by a damascene process[23] (figure 4). Electron mobility degradation is reported compared to SiO2 gate dielectric[23] attributed to stress induced phonon scattering. These materials have a smaller bandgap than SiO2: thus trapping is a strong reliability issue. That is why a SiON interface could be helpful to reduce the leakage current thanks to the higher bandgap of SiON.

4.3) Architectures Alternatives to improve CMOS performances and integration density.

In order to obtain the lowest subthreshold slope(60mv/dec) and acceptable DIBLon FDSOI a practical rule is used: $T_{Si} \acute{U} L_{gate}/4$[29]. The spreading of potential into the buried oxide, due to the coupling with the top gate, increases the coupling between source and drain and thus DIBL. Ultra-thin SOI films are difficult to control. That is why partially depleted SOI has been proposed[29,30]. Because of complete isolation of the SOI devices as well as lower junction capacitance, improved figures of merit are obtained as compared to bulk[29]. The threshold voltage is dependent on Si film thickness whenever the film thickness becomes lower than the space charge region. VT is expressed as[29]:

$$V_T = V_{FB} + 2\varphi_F + \frac{qN_A T_{Si}}{2C_{ox}} \quad (7)$$

N_A is the acceptor concentration; T_{Si} is the silicon thickness; C_{ox} is the gate insulator capacitance.

Scaling of FD devices encounters some limitations due to the quantum confinement in ultra thin films and its incidence on the threshold voltage value[31]: the increase of the fundamental level of the conduction band will increase flat band voltage and VT consequently.

Recently, the functionality of ultra small 6nm gate length devices on 7nm thin Si film was demonstrated[32].

Self-heating is an issue on fully isolated devices because of bad SiO2 thermal conductivity. Replacing SiO2 by Al2O3 has been proposed as a solution because the thermal conductivity of Al2O3 is ten times larger than for SiO2[33],[34]

SOI material should allow to realize attractive devices like multi gated MOSFETs[35] that will allow further scaling of FD depleted devices which are limited by the quantum confinement issue and DIBL via the coupling of the gate with buried oxide [31]. With multi gate devices, short channel effects and leakage current can be drastically reduced because 60mV/dec subthreshold swing and high drivability can be obtained. Transport occurs by volume inversion due to the coupling of both gates. The conditions to control short channel can be relaxed compared to single gate FD devices[31][36], [37],[38],[39],[40]. Nevertheless, the control of thin SOI and design of high density circuits with these devices have to be demonstrated.

The main feature of these devices is to bring a solution to the channel dopant fluctuation problem. Reducing the film thickness to the minimum, allows to use nearly intrinsic Si films because bulk punch-through is no more a problem. Adjusting VT to match overdrive with a low supply voltage will require to adjust the gate workfunction φ_M according to relation (3.1). That is why, workfunction engineering on metal gate and HiK stacks is mandatory for low VS applications.

4.4 Source and drain engineering.

Low energy (<1keV)[25] and heavy molecules (BF3[41], B10H14[42],...)are the easiest ways to replace Boron to achieve p+ shallow junctions. Plasma doping is investigated as an alternatives to obtain lower than 25nm as implanted p+ junction depths[43]. Transient Enhanced Diffusion (TED) is still limiting process to reach the specified final

junction depths. Fast ramp up and down -so called spike annealing- must be combined with Low Energy Ion Implantation [43] to reduce TED as much as possible, by reducing the role played by extended and dopant defects. Excimer Laser Anneal[44],[45] has demonstrated the best trade off between low sheet resistance and junction depth shallowness: highest solid solubility combined with fast processing can be achieved. Low sheet resistance combined with low silicon consumption can be obtained with monosilicides(NiSi,PtSi,) instead of disilicides (TiSi2, CoSi2)[46]. Devices on thin SOI will require raised sources and drains to facilitate silicidation.

5. ALTERNATIVE CMOS OR ALTERNATIVE TO CMOS?

Many research teams are making efforts on Single Electron Transistors(SET)operation based on the Coulomb blockade principle. Demonstration of CMOS inverter operation at 27K has been achieved by using a Vertical Pattern Dependent Oxidation (V-PADOX) process[47]. No solution has been found that could compete with CMOS devices. Some possibilities to achieve memory functional devices by using single electron trapping by a Coulomb blockade effect for DRAM [48], or Non Volatile applications[49], [50], [51]. have been pointed out. This effect supposes that the Coulomb energy $\frac{e^2}{2C}$ (8) is larger than the thermal energy of electrons kT(e is the electron charge; C is the capacitance of the quantum box). This energy is necessary to localize electrons in a Coulomb box provided that tunneling is the limiting process: implicitely, one has to use very low capacitance and sufficiently high tunneling resistance. However, the Coulomb blockade process will be self limiting by charge repulsion which reduces the speed of the charge transfer. Non Volatile Memory applications can be envisaged by using trapping in nanometer size Si quantum dot[50]: Al2O3 has been chosen as the tunnel insulator with reasonable interface states density(less than 10^{11} cm^{-2}) and can also increase the dot density as compared to other materials(in the range of $10^{12}cm^{-2}$).

Whether the involved writing or erase mechanisms are due or not to single electron transfer has been a controversial debate. If the Si dots are randomly distributed in large area devices then it is very difficult to identify whether the single electron transfer is occurring or not due to the large number of dots. It is thus very important to use a device of the smallest size possible to get a high sensitivity to single electron transfer in one dot or a low number of dots. Such a result has been obtained at room temperature on 20nmx20nm Non Volatile Memory Silicon wire based on Silicon quantum dots(Figure 5a)[51]: current spikes on the writing or erasing characteristics have been identified as single electron trapping or detrapping respectively. Coulomb blockade oscillations can be observed if the series access resistance with the quantum well is high enough compared to the resistance quantum $(\frac{e^2}{h})^{-1}$ [52] (9). This effect has already been reported on 50nm gate length N channel MOS transistors at 4.2K[53] making CMOS transistors attractive as single electron devices candidates. As gate length is scaled down to 20nm, access resistance becomes larger and channel conductance oscillations appear at higher temperatures(here 75K) (figure 5b) [4].

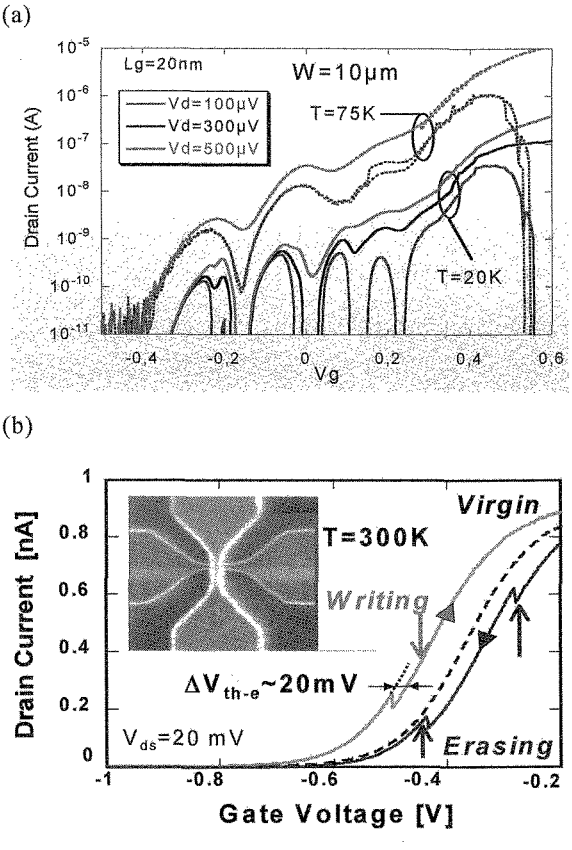

Figure 5 Devices characteristics evidencing Single Electron phenomena (a) Drain current oscillations in a Lg=20nm MOSFET at 75 and 20K, demonstrating that Coulomb blockade is possible in such devices[3] (b) Writing and erase characteristics of 20nmx20nm(WxL) devices at room temperature. Spike in Id(Vg) characteristics is due to trapping or de-trapping of one electron in SOI nanowire Si dot Memory. Top view of 20nmx20nm nanowire[10] inserted.

6. CONCLUSIONS

Beyond the roadmap, multigate devices using strained channels will be widely used for high performance CMOS. Si based alloys or compatible semiconductors will be introduced to enhance the possibilities of future Systems on Chip. Single electronics will be a major study subject to optimize the use of ultra small devices.

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