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Self-aligned FinFETs with Wide Source/Drain Regions

Byung-Gook Park, Dong-Soo Woo and Jong Duk Lee

Inter-university Semiconductor Research Center (ISRC) and
School of Electrical Engineering and Computer Science, Seoul National University
Shinlim-dong, Kwanak-gu, Seoul 151-742, Korea
Fax: 82-2-882-4658, e-mail: bgpark@snu.ac.kr

Self-aligned FinFETs with wide source/drain regions were fabricated. The gate length of FinFETs was about 30nm and the fin thickness was about 20nm. 3.6nm gate oxide was grown on (110) channel. Drain current was 330 μA/μm and transconductance was 650 μS/μm at a gate overdrive of 0.8V, which is somewhat low due to the thick gate oxide. In spite of the thick gate oxide for 30nm device, short channel effect of our FinFETs is suppressed sufficiently, which is the advantage of double-gate MOSFETs. In addition, reduced short channel effect may be caused by the non-uniform source/drain doping profile inherent in our devices. This structure can be used for low power application. As the source/drain doping is performed before gate formation, it is also compatible with metal-gate FinFET process.

Key words: low resistance, nanoscale, self-aligned FinFET, non-uniform junction

1. INTRODUCTION

As CMOS dimensions shrink down into a few tens of nanometer regime, the planar CMOS structure shows its limitation due to the source-to-drain leakage current. To suppress this current, high channel doping is unavoidable. Thus, planar CMOS devices can suffer from mobility degradation and dopant fluctuation.

Fully-depleted(FD) SOI MOSFET and double-gate(DG) MOSFET can suppress short channel effect without using high channel doping. These devices are considered to be a candidate for post planar CMOS device structure in ITRS2001. They can avoid mobility degradation and dopant fluctuation problem. Among them, double gate MOSFET structure shows the possibility of further scaling down to 10nm regime.

There are three groups of double-gate MOSFET. They are classified according to gate and channel position. Planar DG MOSFET and vertical MOSFET have disadvantages due to its process complexity.

FinFET[1] is probably the most promising DG device structure due to its process compatibility with planar process. In experimental level, FinFETs with a gate length of 10nm have been reported[2].

To suppress short channel effect in FinFETs, the fin width should be less than 0.7 times the gate length[3]. However, conventional FinFET structures would not have the best performance

due to the structural weakness that ultra thin channel is used as a part of source/drain region. This can cause the increase of parasitic resistance and degrades the drive current. To fabricate devices with low source/drain extrinsic resistance, the source/drain fan-out region should be wide and the length of the ultra-fine channel region which act as a source/drain should be as short as possible. Y. Choi[4] and J. Kedzierski[5] proposed device structures which have large source/drain fan-out region using selective Ge deposition or selective epitaxy process.

In this paper, we propose and fabricate a novel FinFET structure with wide single crystalline silicon source/drain fan-out region. Wide source/drain region is connected to the ultra-fine channel at the gate edge in a self-aligned manner.

2. FABRICATION

The self-aligned FinFET process is shown in Fig. 1. Starting material was $1x10^{15}$ cm^{-3} boron doped (100)-oriented SOI wafer. Top silicon layer was thinned to 100nm using thermal oxidation and stripping. To protect the fin region, a-Si/SiO_2 stacked channel hardmask was defined on top of the device active region using e-beam lithography and dry etching (Fig. 2(a)). Then, 50nm TEOS oxide spacer was formed along the channel hardmask to provide smooth surface for later lithography and to guarantee sufficient spacing between the channel and the implanted region. Arsenic was implanted at energy of 20keV to form source/drain at a dose of $2x10^{15}$ cm^{-2}. 100nm oxide was deposited and, by using e-beam lithography and subsequent sequential etching of oxide and 50nm SOI layer, grooves were formed across the channel hardmask. Source/drain region was separated except the fin as shown in Fig 1(d). Sacrificial oxidation was performed at a condition of 5nm oxide growth on (100) silicon surface. The oxide was removed and 3nm gate oxide was grown. Poly-silicon layer was deposited using LPCVD at 625°C and doped with $POCl_3$. As the width of groove is smaller than the thickness of gate polysilicon layer, subsequent etchback of polysilicon results in the gate electrode filled in the region of groove in a self-aligned manner. Source/drain doping profiles were diffused to the fin edge by an additional heat treatment. Back-end process including ILD deposition and aluminum metallization was performed without silicidation process.

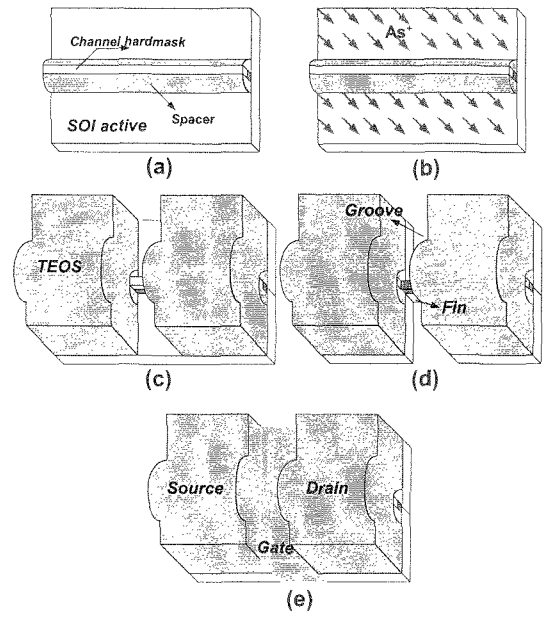


Fig 1. Key process sequence of self-aligned FinFET consists of (a) channel hardmask and oxide spacer formation, (b) S/D doping, (c) groove formation, (d) SOI etching outside fin, and (e) gate electrode deposition and etchback.

Fig. 2 shows the SEM view taken after groove and SOI etch as in Fig. 1(d). The groove width was about 30nm and the fin thickness was 30nm.

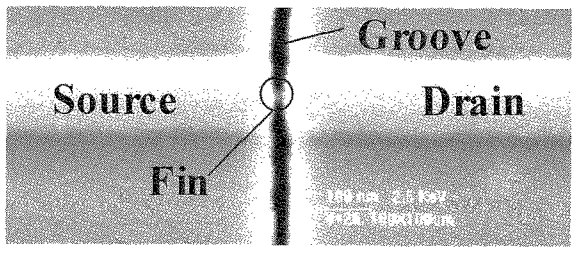
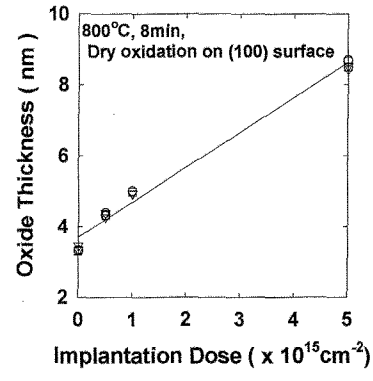


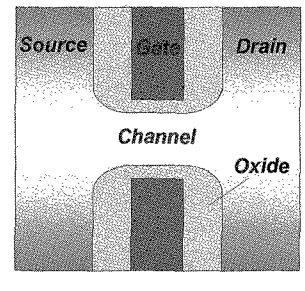
Fig. 2. SEM micrograph of the device after silicon etch as in Fig. 1(d). 30nm groove width and 30nm channel thickness can be obtained from the 55nm and 50nm drawn patterns.

Groove width reduction was observed due to the height difference between active region and channel hardmask region. As the sacrificial and gate oxidation processes were on (110) surface of silicon, the grown oxides should be thicker than (100) surface. Assuming enhancement factor of 1.2, the estimated final fin width and groove width will be 22nm and 32nm, respectively. As the doping concentration where the gate overlaps with the source/drain region is high, different oxide thickness can be obtained as shown in Fig. 3.

Thicker gate-to-source/drain oxide can prevent any tunneling leakage that may occur at gate-to-source/drain surface and reduce overlap capacitance between source/drain and channel. In addition, the doping dependent oxidation provides a nice flare-out region between the narrow channel and the wide source/drain region as shown in Fig. 3(b)



(a)



(b)

Fig. 3. (a) doping dependency of thermally grown oxide thickness. (b) shows the plan view of device. Gate-source or gate-to-drain oxide thickness is thicker than gate-to-fin oxide.

3. RESULTS

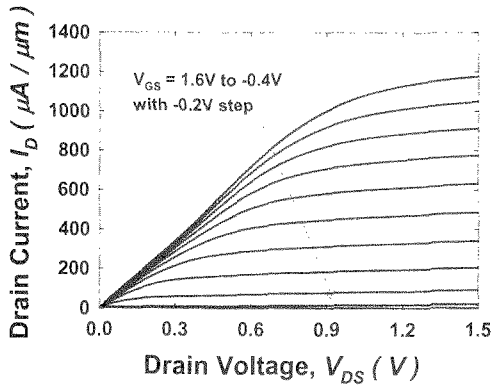
Electrical characteristics of fabricated devices were measured using HP4155A. Threshold voltage was defined as the gate voltage when drain current becomes 100nA per unit device width.

Fig. 4 shows output characteristics and subthreshold characteristics of a fabricated device. In this device, as p-type channel doping was $1x10^{15}cm^{-3}$ and the gate silicon was n^+ polysilicon, the threshold voltage remains negative.

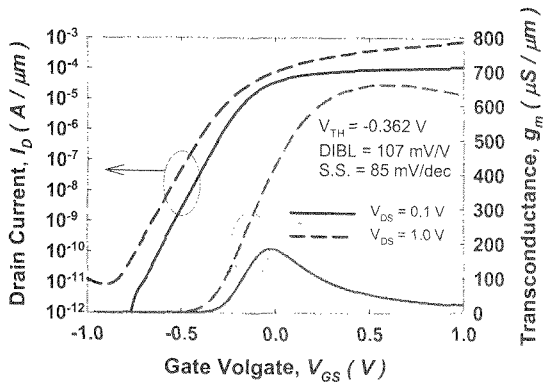
However, DIBL and subthreshold slope values were reasonable in spite of relatively thick (3.6

nm on the channel surface) gate oxide and low channel doping.

Drain saturation current and transconductance were 330 μA/μm and 650 μS/μm for 0.8V gate overdrive, respectively. (For the channel width, we used 2x(fin height), considering the nature of double gate structure.) This somewhat low performance was due to thicker gate oxide and high source/drain contact resistance whose value was 1.15kΩ measured from the Kelvin pattern.



(a)



(b)

Fig. 4. Measured (a) output characteristics and (b) subthreshold characteristics. Gate length was 32nm and fin width was 22nm. Gate oxide was 3.6nm on (110) surface.

Fig.5 shows DIBL and subthreshold swing values of fabricated devices with various drawn channel thickness and groove width.

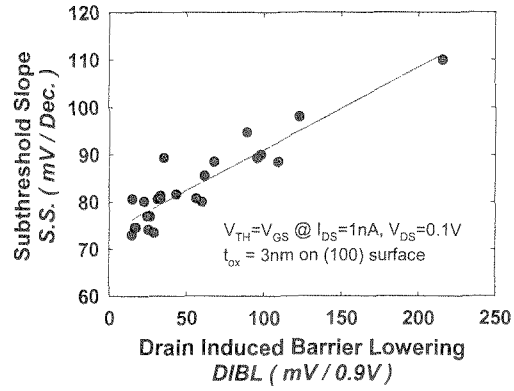


Fig. 5. Subthreshold swing and DIBL for the fabricated devices. Though relatively thick gate oxide, short channel effect was suppressed appropriately.

According to general scaling rule of double gate MOSFET, subthreshold swing of 100mV/dec can be obtained when parameter α_2 is equal to 2[3]. For 3.6nm gate oxide and 32nm gate length, required fin width is about 21nm, which is similar to the estimated fin width of 22nm. Further reduction of short channel effect in these devices can be explained by the reduction of critical dimensions such as fin width and gate length in the fabricated devices.

Another reason was non-uniform source/drain doping profile. Vertically non-uniform doping profile[6] and lateral non-uniform doping along the fin width direction inherent in our device can contribute to the reduction of short channel effect. To explain this, we performed 2-dimensional device simulation. Fig. 6 shows channel potentials of 2 types of devices, which have uniform and non-uniform lateral doping profile along fin widths direction. Non-uniform device

shows less drain field penetration at the channel center, which means reduced short channel effect.

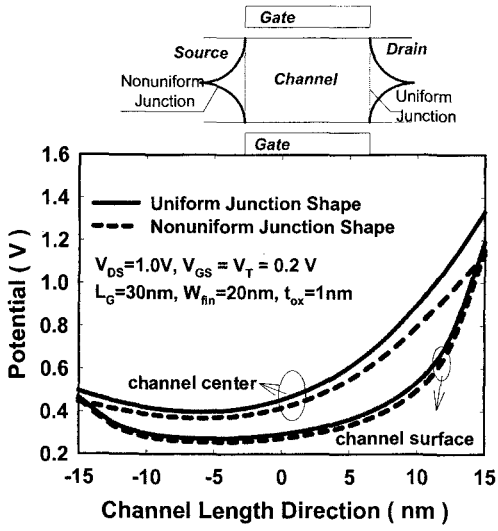


Fig. 6. Simulated channel potential for the devices with different source/drain junction shape along the fin width direction. Non-uniform junction reduces the drain field at the channel center.

4. CONCLUSIONS

We fabricated a novel self-aligned FinFET device whose gate is located at the edge of wide single crystalline source/drain fan-out region. Short channel effect was properly suppressed with 3.6nm gate oxide. Drain saturation current and transconductance were 330 μA/μm and 650 μS/μm at 0.8V gate overdrive despite the relatively thick gate oxide. If we can make thinner gate oxide, device performance can be improved. Additional margin in short channel effect can be obtained from non-uniform source/drain doping profile.

This device can be used for low power application and due to the pre-source/drain process sequence, it can be compatible with metal gate FinFET.

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