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Analysis of New SOI Materials and Advanced SOI MOSFETs

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Recent experimental data and simulation results on state-of-the-art SOI structures are reported, demonstrating the key role of the device dimensions: thickness of the buried oxide, gate oxide, and silicon film. Thickness scaling and MOSFET miniaturization give rise to a number of critical issues. The analysis of self-heating problems in SOI MOSFETs suggests the replacement of the buried oxide with a different dielectric that offers improved thermal conductivity. The Gate-Induced Floating Body Effects (GIFBE) are described and shown to depend on the device geometry and measurement conditions. In ultra-thin SOI films, the coupling effects are amplified leading to interesting consequences. The operation principles and merits of transistors with 3 or 4 gates are discussed.
Key words: SOI, MOSFET, FBE, pseudo-MOS

1. INTRODUCTION

The limits of the conventional CMOS scaling become visible and generate renewed interest in Silicon On Insulator (SOI) technology [1-3]. SOI is adopted by major companies for the fabrication of high performance processors and low-voltage/low-power circuits. However, in order to break the 10-nm MOSFET barrier, new SOI-like materials and advanced concepts for transistor architecture are needed. The aim of this paper is to review the future trends and discuss very recent experimental results on advanced SOI structures. The paper is organized in four sections. Section 2 is dedicated to the electrical properties of ultra thin film SOI wafers, measured with the pseudo-MOSFET technique. In section 3, it is shown that the body of the MOS transistors can be charged by tunneling currents, giving rise to remarkable gate-induced floating body effects. The giant coupling effects between the two channels, observed in sub 10-nm-thick SOI transistors, are presented in section 4. Finally, section 5 describes the operation and properties of SOI transistors with more than two channels.

2. INNOVATIVE SOI MATERIALS

The possibility to scale down the thickness of the Si film and buried oxide (BOX) is the main attribute of SOI transistors for complying with the ITRS constraints [2,3]. Film thinning below 10 nm can be achieved by sacrificial oxidation, which is much easier if the starting SOI wafer is already thin. The quality of the film, BOX and interface is evaluated with the pseudo-MOSFET technique [1]. The main parameters that can be extracted are the carrier mobility and lifetime, concentration of BOX charges and interface traps, threshold and flat-band voltages. Figure 1 shows that the carrier mobility is lower in 10 nm thick films than in standard 200 nm films [4]. However, the mobility and lifetime (not shown) can be `repaired' by epitaxial regrowth. This implies that the defects induced by aggressive thinning are eliminated or dispersed during regrowth [4].

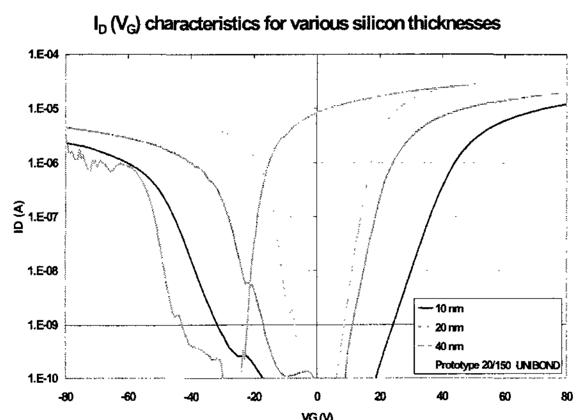

Figure 1. Pseudo-MOSFET drain current versus gate voltage $I_D(V_G)$ characteristics in SOI wafers with silicon film thinned down to 10 nm and epitaxially regrown to 20 and 40 nm (after Allibert *et al* [4]).

The current demand for thinner BOX (below 50 nm) is motivated by two arguments: reduction of the short-channel effects induced by the lateral fringing fields [5] and improvement of the thermal dissipation. Counter arguments are the stronger coupling between the front and back channels and the susceptibility to substrate effects (increased capacitance, depletion underneath the BOX which increases the effective oxide thickness, impact of the more defective bonded BOX-substrate interface). The scaling of the BOX is therefore a matter of trade-off: thinning is unavoidable, whereas too much thinning is detrimental.

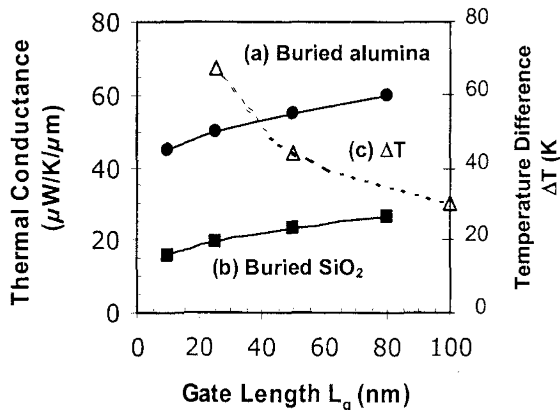

Figure 2. Thermal conductance versus channel length in SOI MOSFETs with SiO_2 BOX (a), alumina BOX (b), and corresponding temperature difference (c). Parameters: 10nm film, 100 nm BOX (after Oshima *et al* [6]).

A different avenue in SOI material science is to replace the buried oxide with a different dielectric that offers improved thermal conductivity. Figure 2 demonstrates that self-heating, mainly due to the poor thermal conductivity of the SiO_2 BOX, can be remarkably attenuated in alumina-based SOI wafers. Note that the resulting material is still SOI-like - thin Si-film, high-K dielectric, Si substrate - and can be synthesized by adapting the Smart-Cut process. 2-D simulations of scaled SOI MOSFETs show that the temperature in the channel can be reduced by about 50°C, just by replacing the BOX with buried alumina [6]. Since the mobility varies as $T^{-1.5}$, the gain in mobility and speed can reach 25-30%. This gain corresponds to the expected benefit of one-step down scaling and also compares well with the promises of strained silicon.

3. GATE-INDUCED FLOATING BODY EFFECTS

The scaling of the gate oxide results in new MOS effects enabled by the gate tunneling current. In particular, the body of the SOI transistors can be charged by the tunneling currents, giving rise to gate-induced floating body effects (GIFBE) [7]. Since the body is no longer charged by impact ionization, the novel mechanism occurs even at low drain voltage. GIFBE is responsible for significant changes in transconductance, which exhibits a second peak as shown in Figure 3.

The raise in body potential is governed by the balance of body charging (via tunneling) and body discharging (by junction leakage and carrier recombination). This explains the dependence on the gate size and scanning mode (speed and direction) [7]. The amplitude of GIFBE decreases in shorter (Fig.3) and narrower MOSFETs. Longer the measurement time, lower the gate voltage necessary to trigger GIFBE.

Different models apply to partially and fully depleted SOI MOSFETs. In partially depleted devices, the increase in body potential lowers the threshold voltage and increases the drain current. In fully depleted MOSFETs, GIFBE modifies the potential at the back film-BOX interface; the interface coupling effect leads to the lowering of the front-channel threshold voltage [8].

GIFBE is responsible for excess Lorentz noise (superimposed on the conventional 1/f noise [9]) as well as for a remarkable attenuation of the transient effects (drain current overshoot and undershoot) [7]. The impact on history effects is also very important for circuit applications.

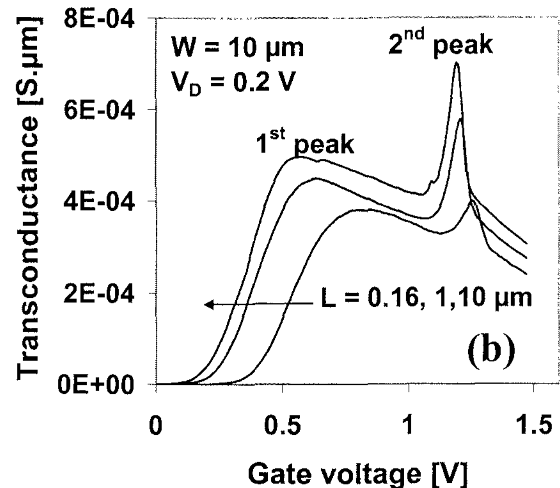

Figure 3. Normalized transconductance versus gate bias for different channel lengths (after Cassé *et al* [8]).

4. ULTRA THIN BODY EFFECTS IN SOI MOSFET

The thinning of the silicon films is the most efficient strategy for scaling down SOI MOSFETs [2,3]. If the threshold voltage is well controlled by the use of gate materials with appropriate work-function, the film can be left undoped in order to preserve high carrier mobility.

In thin fully-depleted films, the interface coupling effects are amplified. According to Lim and Fossum [10], the threshold voltage of the front channel decreases with increasing the back-gate voltage and vice-versa. It is possible to draw both characteristics $V_{T1}(V_{G2})$ and $V_{G1}(V_{T2})$ on the same graph. In general, the two curves are different and intersect in point X. This point indicates the unique couple of front and back gate voltages that guarantees the simultaneous activation of the two channels.

However, in sub 10 nm thick films, the two curves can be superposed (Figure 4) [11]. This means that an arbitrary back-gate bias V_{G2} is promoted as threshold voltage as soon as the front gate is biased at threshold. In other words, when the front channel reaches strong inversion, the back channel is also dragged into inversion. This giant coupling results from the profile of the body potential which is rather constant between the two gates (rectangular well).

The coupling effects are important because they show the degree of susceptibility of the front channel to remote defects (located in the BOX or at its interfaces), fringing fields, and radiation events. This coupling must be correctly accounted for when a regular single-gate SOI MOSFET is emulated in double-gate mode. The proper bias conditions for virtual double-gate operation depend on film thickness: intercept point X for thin films and any point situated on the curve of Figure 4 for ultra-thin SOI films [11].

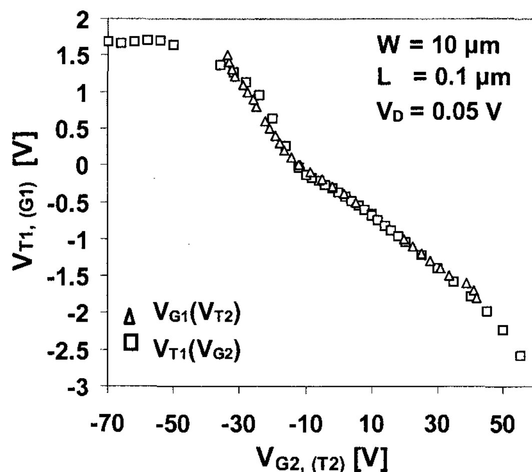

Figure 4. Giant coupling effect: $V_{T1}(V_{G2})$ and $V_{T2}(V_{G1})$ in 9 nm thick SOI MOSFETs (after Pretet *et al* [11]).

5. SOI MOSFET WITH MULTIPLE GATES

Double-gate, triple-gate and four-gate transistors have recently been proposed for enhanced performance and functionality. Since several channels and conduction mechanisms are simultaneously activated, their separation and characterization are very challenging.

The mobility behavior in double-gate MOSFETs attracts large interest [12]. Measurements and simulations have shown that volume inversion results in a higher mobility than in single-gate transistors. In addition, the carrier mobility is expected to reach a maximum in 3-5 nm thick films, where the influence of surface roughness scattering is minimized [12,13].

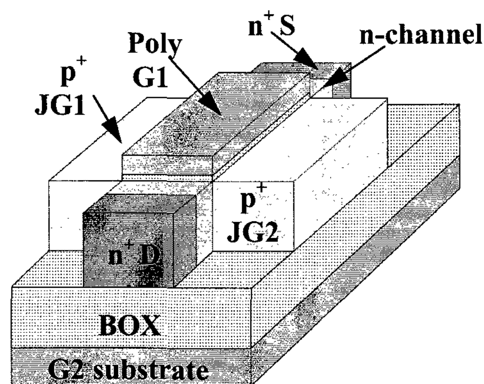

Figure 5. Schematic configuration of n-channel G^4-FET (after Akarvardar *et al* [16]).

In FinFETs, the gate can activate three channels. The role of the top channel prevails if the body width (inter-gate distance) exceeds the fin thickness. Comparing transistors with various aspect ratios, it was found that the carrier mobility is clearly degraded on the fin edges [14].

The four-gate transistor (G^4-FET) is operated in accumulation-mode and has the same structure as an inversion-mode SOI MOSFET with two body contacts. The current flows between these body contacts which play the role of source and drain (Fig.5) [15]. The G^4-FET has the standard front and back MOS gates plus the two lateral junctions that control the effective width of the body. The conductive path is modulated by mixed MOS-JFET effects: from a tiny quantum wire, surrounded by depletion regions, to strongly accumulated interface channels. Each gate has the capability of switching the transistor on and off [16]. The independent action of the four gates opens new perspectives for mixed-signal applications, quantum wire effects, and quaternary logic schemes.

6. CONCLUSION

SOI wafers and devices already play a vital role in the CMOS technology, where SOI provides enhanced capabilities. The future of SOI is even brighter, as device scaling will be blocked without SOI-like structures. The evolution of the MOS transistor will be continued by shrinking the dimensions of the body, gate oxide and BOX. The nature of the various layers will also be reconsidered in order to infuse new functionality and performance. The transistor architecture will rapidly evolve to multiple gate configurations. We have attempted to call attention on these exciting trends and have pointed out several new mechanisms that become important.

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