Transactions of the Materials Research Society of Japan 29[4] 1365-1368 (2004)

Structural and Electrical Properties of $Bi_{4-x}La_xTi_3O_{12}$ Thin Films Formed on p-Si(100) Substrates

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Crystallization of sol-gel derived $Bi_{4-x}La_xTi_3O_{12}$ (BLT) thin films deposited on p-type silicon substrates and their interface structures have been investigated by means of X-ray diffraction (XRD) and X-ray reflection (XRR). When the annealing temperature is higher than 550 °C the film was crystallized into bismuth-oxide layered perovskite structure for one hour. In the case of 550 °C, the crystallization from amorphous phase and the grain growth mostly took place until 120 min. From analysis of XRR spectra by simulation fitting the thickness and the density of the BLT layer after two hours annealing at 550 °C are evaluated to be about 66 nm and 7.2 g/cm^3, respectively. Also, it was indicated that a 3.4 nm-thick interfacial layer was formed between BLT and Si. The average crystal dimension in the polycrystalline film annealed for 2 hours at 550 °C was estimated to be about 60 nm by Scherrer equation. Hysteresis in capacitance-voltage characteristics of the Au/BLT/p-Si structures was observed, and the hysteresis voltage width had a tendency to increase and to be saturated with increasing the gate voltage. The dielectric constant of the BLT layer was evaluated to be as low as 17.

Key words: ferroelectric thin film, $Bi_{4-x}La_xTi_3O_{12}$ (BLT), crystallization, X-ray reflectivity analysis, metal-ferroelectric-semiconductor structure

I. INTRODUCTION

Ferroelectric thin films have been widely researched for non-volatile random-access memory applications. Some kinds of films of bismuth layer-structured ferroelectrics, such as $SrBi_2Ta_2O_9$ (SBT), $Bi_4Ti_3O_{12}$ (BIT), $Bi_{4-x}La_xTi_3O_{12}$ (BLT), are recognized as the materials which are promising candidates for the memory applications because of their excellent fatigue-free and lead-free natures [1-3]. Recently, BLT thin film has been reported as a fatigue-free material which can be formed at lower temperature than SBT ferroelectric thin films [3]. The effect of substitution of La and/or V in BIT thin films and the electronic structure of BLT have been studied [4, 5]. Also, properties of BLT polycrystalline thin films fabricated by chemical solution decomposition method have been reported [6, 7].

A metal-ferroelectric-semiconductor (MFS) structured type memory has advantages compared with the storage capacitor-type memory because of the non-destructive read-out and device scaling capabilities. It is essential for the development of the MFS field-effect transistor (FET)-type memory to understand the crystallization, the electric properties of the thin films formed on silicon substrates, and the ferroelectric/silicon interface properties which affects seriously on the FET characteristics. The electrical characteristics of the BIT thin films on silicon substrates or insulator/silicon substrates have been investigated [8-12] but the control of the device characteristics is not sufficient.

In order to control electrical characteristics of the BLT thin film on Si substrate, we investigated the crystallization of sol-gel derived BLT thin films (thickness < 100 nm) and the interface structure between BLT and Si. Furthermore, the electrical characteristics of the BLT film on Si substrate were also evaluated.

2. EXPERIMETNAL

For hydrogen termination of silicon surfaces p-type Si(100) wafers were treated in a diluted HF solution for 60 s after a chemical cleaning. A sol-gel precursor solution was deposited on the Si substrates by spin-coating technique. Immediately after solution coating the wafers were dried on a hot-plate at 150 °C for 30 min. Subsequently, the samples were annealed at temperatures of 500-700 °C in a furnace for crystallization.

X-ray diffraction and reflection measurements were carried out by means of the same diffractometer (Philips: X'Pert PRO system) with the graded multilayer mirror for thin film analysis. Incident X-ray (CuKα) is converted from the divergent beam into a quasi-monochromatic and –parallel beam of high intensity by the mirror, and the diffracted or reflected X-ray was detected through the slits and the graphite monochromator in front of the detector. XRD measurements were carried out under the condition that the glancing angle of the incident beam from the surface is fixed at 5 degrees and the detector was scanned (2θ scan). Analysis of XRR spectrum was carried out by model calculation and fitting to the data [13]. For the measurement of capacitance-voltage and current-voltage

characteristics of the MFS structures gold electrodes were fabricated on the film by evaporation. All the measurements were carried out at room temperature.

3. RESULTS AND DISCUSSION

3.1 Crystallization of BLT thin film on Si substrate

X-ray diffraction profiles as a function of annealing temperature for the annealing time of 60 min are shown in Fig. 1. When the annealing temperature was 500 °C no diffraction from the crystal was observed and thin film was solidified into amorphous. As the annealing temperature higher than 550 °C the diffraction from the Bi-layered structure was clearly observed. On the other hand, at 700 °C the peaks which did not assign to the BLT structure were observed.

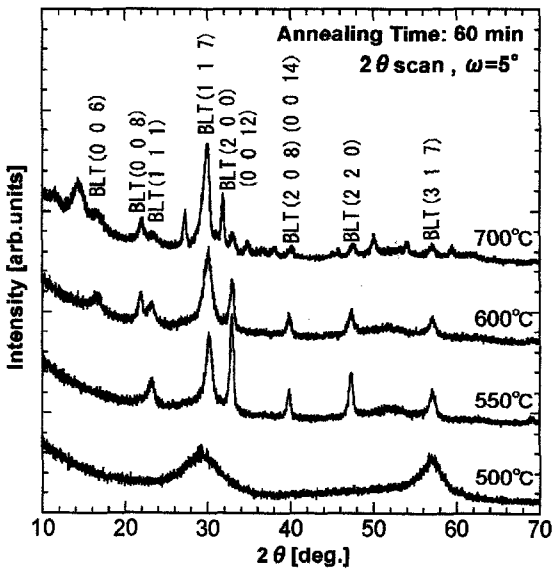

Fig. 1 Annealing temperature dependence of XRD profile. The annealing time was 60 min.

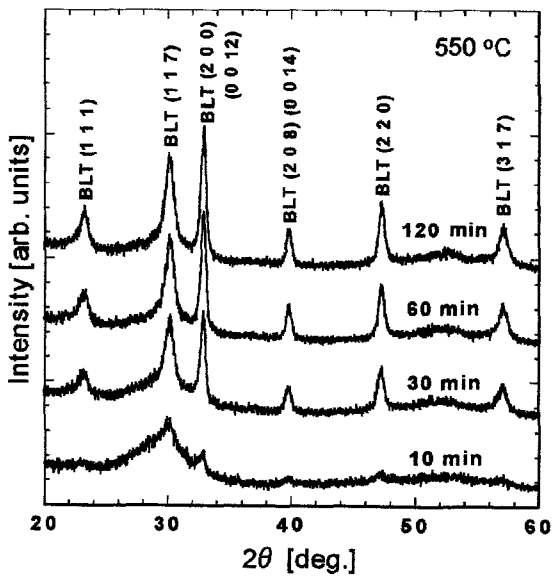

Fig. 2 Annealing time dependence of XRD profile. The annealing temperature was 550 °C.

For the crystallization at 550 °C the time dependence of XRD profile has been investigated as shown in Fig. 2. After 10 min annealing, the broad scattering and the small peaks from the crystals were observed. This means that the crystallization has already started at 10 min but the film consists of a large amount of amorphous and small crystals. The diffraction peaks were dramatically increased for 30 min annealing. Figure 3(a)-(c) show the annealing time dependence of the integrated intensity, the peak intensity and the full-width half maximum-intensity of the diffraction peaks, respectively. The integrated intensities mostly increased until 60 min and were almost saturated during 120 min. This indicated that the transformation from amorphous into the crystal fast occurred until 60 min and almost finished until 120 min. The intensities were increased and saturated, and the widths of the peaks are decreased and saturated with annealing time, as show in Figs 3(b) and 3(c). These results mean that the grains grew larger simultaneously with the crystallization. During annealing the peak positions (2θ) shifted to higher angle, as shown in Fig. 4. This resulted in the decrease of the lattice constant during annealing. The crystal dimensions in the polycrystalline BLT thin films were evaluated from the narrowing of the peak width by using Scherrer equation after subtraction of the contribution of the optical character. The average crystal dimension was about 60 nm for the film annealed at 550 °C for two hours. This size is comparable to the film thickness evaluated from XRR analysis as described below.

The measured and simulated spectra of XRR from the thin films on Si were shown in Fig. 5 as a function of annealing temperature. The simulation fitting [15] was carried out by using the three layer model with roughness, as also shown in Fig. 5. The intensity oscillation is caused by the interference between the X-rays reflected from the surface and the interface. The amplitude of the oscillation decreased with annealing time, indicating that the surface and interface roughness increased with annealing time. The annealing time dependence of the thickness and the density of the layers are shown in Fig. 6(a) and 6(b), respectively. It is found that the thickness of the BLT layer was rapidly reduced and the BLT density increased until 30 min. These changes are related to the crystallization of the film. The increase of the density is consistent with the decrease of the lattice constant as mentioned above. On the other hand, the thickness of the interfacial layer showed a monotonous increase after 30 min. It seems that the formation of the interfacial layer is mainly owing to oxidation of the silicon. The results of the XRR analysis for the sample which crystallized at 550 °C for 2 hours are shown in Table I.

3.2 Electrical Characteristics of Au/BLT/Si structures

Capacitance-voltage characteristics of Au/BLT/p-Si structures were measured at a frequency of 1 MHz, as shown in Fig. 7. Clockwise hysteresis was observed for the BLT film crystallized at 550 °C when the gate bias was swept. The hysteresis voltage width depended on the applied gate voltage as shown in Fig. 8. The hysteresis width has a tendency to be saturated after an increase with increasing the gate voltage. By the

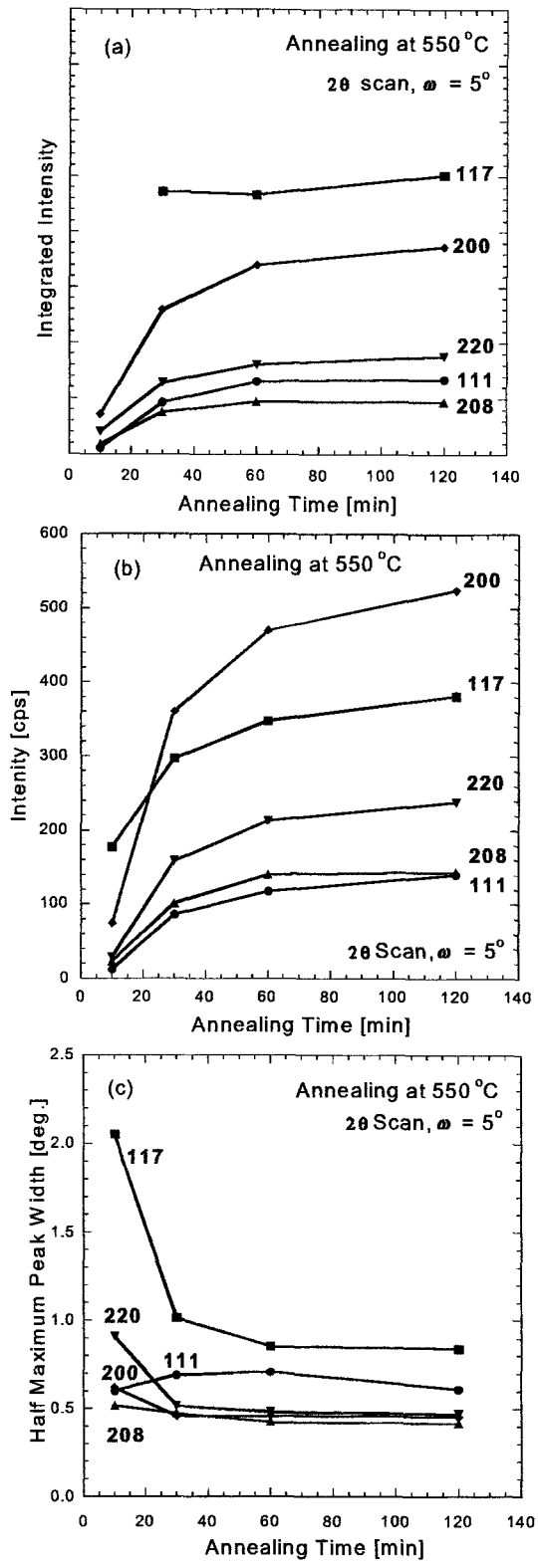

Fig. 3 Annealing time dependence of (a)the integrated intensity, (b)the peak intensity, and (c)the peak width of the diffraction.

calculation using the accumulation capacitance of the MFS structures and the thicknesses of the layers (Table I) the dielectric constant of the BLT layer was estimated to be as low as 17 on the assumption that the interfacial layer was SiO_2.

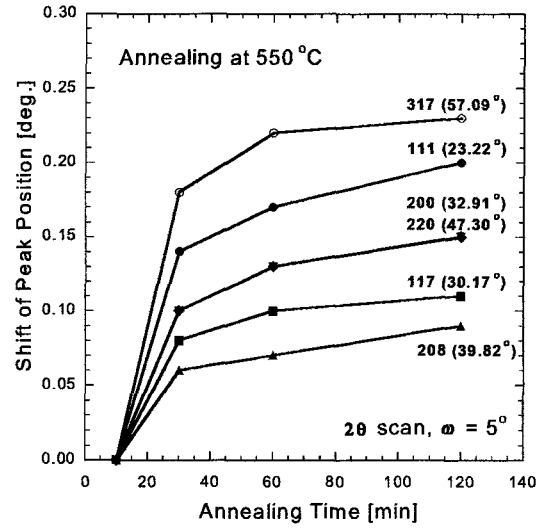

Fig. 4 Annealing time dependence of the shift of the diffraction peak position after 10 min.

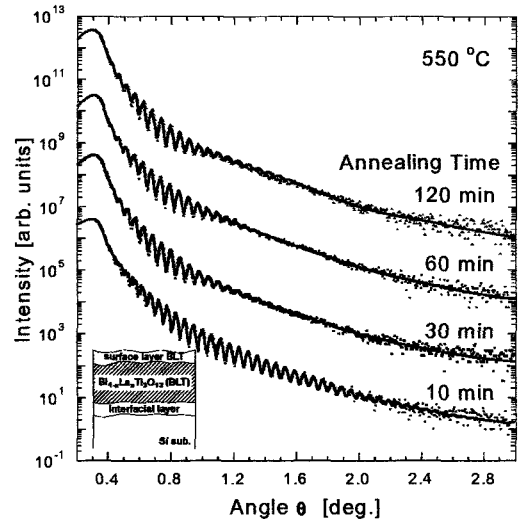

Fig. 5 XRR spectra as a function of annealing time at 550 °C.

Table I The results of simulation fitting for the XRR spectrum of the BLT film crystallized at 550 °C for two hours. The total thickness and the average density of the BLT layer is about 66 nm and 7.2 g/cm^3.

	Thickness [nm]	Density [g/cm^3]	Roughness
surface BLT	2.2	4.4	1.3
BLT	63.6	7.3	1.4
Interfacial layer	3.4	2.5	0.5

4. CONCLUSIONS

Crystallization of sol-gel derived BLT thin films on silicon substrates has been investigated by means of XRD and XRR analysis. When the annealing temperature was above 550 °C the polycrystalline thin film can be formed. It was confirmed that the transformation from amorphous into the Bi-layered

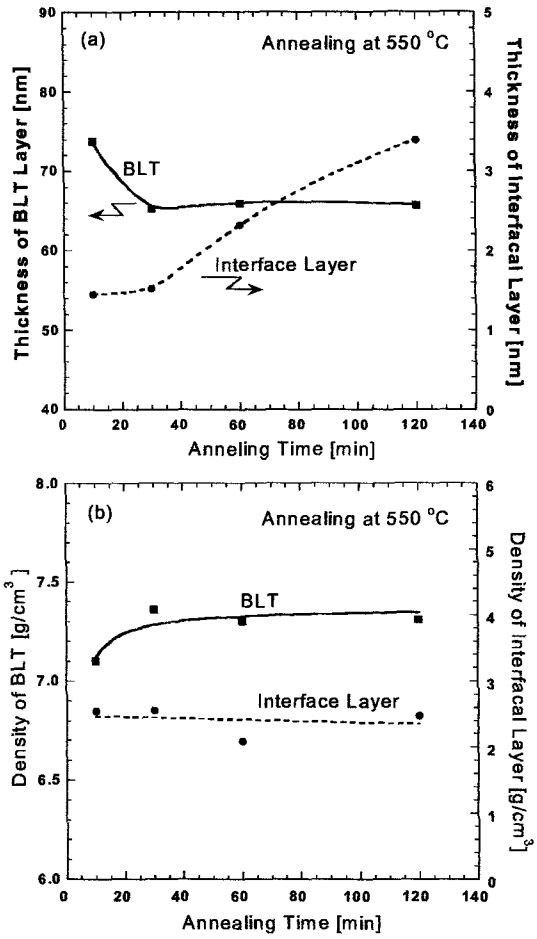

Fig. 6 The annealing time dependence of (a) the thickness and (b) the density of layers at 550 °C.

structure and the grain growth occurred until 120 min with decrease of the lattice constant and increase of the density in the BLT layer. The thickness and density of the BLT layer for the sample crystallized at 550 °C was evaluated by the XRR measurement and the simulation fitting. Also, the average crystal dimension in the BLT film was estimated to be about 60 nm. Furthermore, Hysteresis in C-V characteristics was observed. The dielectric constant was evaluated to be about 17.

Acknowledgements

This work was supported by a Grant-in-Aid for Young Scientists (B) (KAKENHI, No. 14750242) from The Ministry of Education, Culture, Sports, Science and Technology, and also in part by Kitada Shougakkai Kinen Zaidan (No. KEN-03-001).

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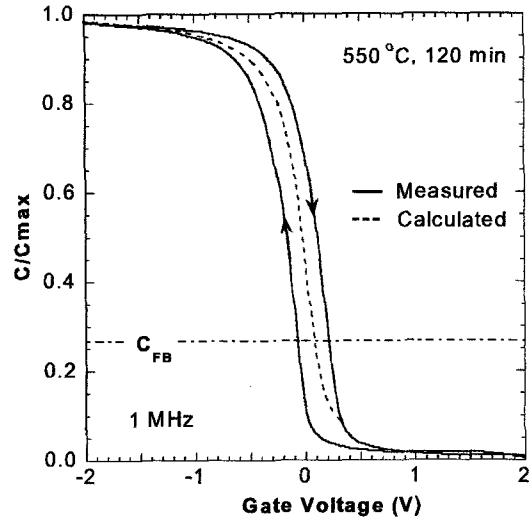

Fig. 7 Capacitance-voltage characteristics of Au/BLT/p-Si structure. The temperature and time of crystallization was 550 °C and 120 min, respectively.

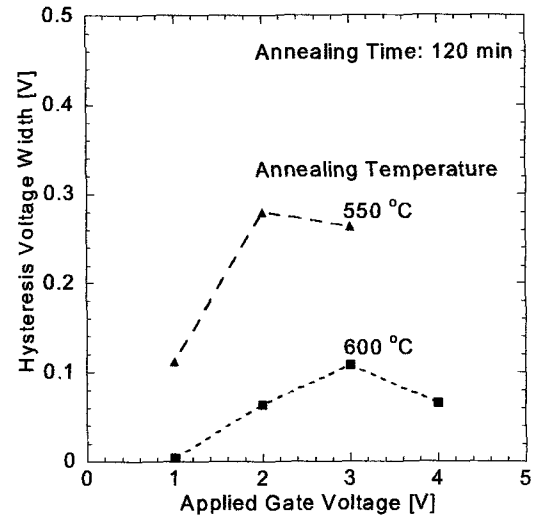

Fig. 8 Hysteresis voltage width of the C-V curves vs. applied gate voltage.

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(Received October 13, 2003; Accepted July 1, 2004)