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The Role of Oxygen-related Defects on the Reliabilities of HfO_2-based High-k Gate Insulators

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The roles of oxygen-related defects on the reliability of HfO_2-based high-k gate insulators are discussed, based on both experimental and theoretical investigations. A large hole current observed under gate negative bias can be attributed to the electron injection from the gate into the defect level due to oxygen interstitials. The hole injection was found to stimulate the release of hydrogen from Si-H terminations, causing of interfacial layer breakdown. Trap-assisted tunneling through defect levels due to the oxygen vacancy ($\mathbf{Vo^{2+}}$) causes SILC in the electron current. An electron trapping-induced energy level shift of oxygen vacancy provides conduction pass for the valence electron, resulting in a substrate hole current increase.

Key words: high-k, HfO_2, reliability, oxygen defect

1. INTRODUCTION

Hafnium oxide-based high dielectric-constant (high-k) films are considered the most promising candidates to meet the requirement for alternative gate insulators. Although their reliability is of great concern, the microscopic mechanisms of degradation are not well understood. Considering the integration of HfO_2-based high-k gate insulator with poly-Si gate CMOSFET, large threshold voltage shifts in pFET is of great concern. It was recently shown that oxygen extraction from HfO_2 to p-Si can occur when HfO_2 is in contact with Si though Hf atoms can bind more strongly than Si atoms to oxygen atoms, and this reaction might be responsible for large threshold voltage shift in pFET with HfO_2 gate insulator [1]. In this paper, the roles of oxygen-related defects on time-dependent dielectric breakdown (TDDB), stress- induced leakage current (SILC) are discussed, based on both experimental and theoretical investigations.

2. DEVICE FABRICATION

Poly-Si gate FETs with HfAlOx or HfSiON gate insulators were fabricated using conventional MOSFET fabrication process flow. After isolation and well formation, an intensive interfacial layer (IL) was formed. In the case of HfAlOx, a nitrogen profile-engineered SiON interfacial layer [2] was used to suppress both inter-diffusion and mobility reduction. HfAlOx thin films were deposited by ALD [3]. Tri-methyl-aluminum, Tetrakis (ethyl-methylamino) hafnium and water were used as precursors. Hf concentration of the film (Hf/Hf+Al) was 30%. For HfSiON, HfSiOx films were deposited by MOCVD using hafnium tetra-t-butoxide (HTB) and Si_2H_6 without oxidant on SiO_2-IL, and then nitrided by N_2/Ar plasma [4]. The Hf concentration of the film (Hf/Hf+Si) was 60%. The EOT of the samples was 1.2 – 2.0 nm. A discussion follows of the reliability of the high-k/SiO_2(SiON) dual layer gate insulator.

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The gate electrode comprised a 150 nm-thick poly-Si. Dopant activation was performed using spike annealing. After metalization, a final sintering anneal was performed in a 3% H_2/N_2 environment for 30 min at 400°C. The TEM photographs of fabricated devices are shown in Fig. 1.

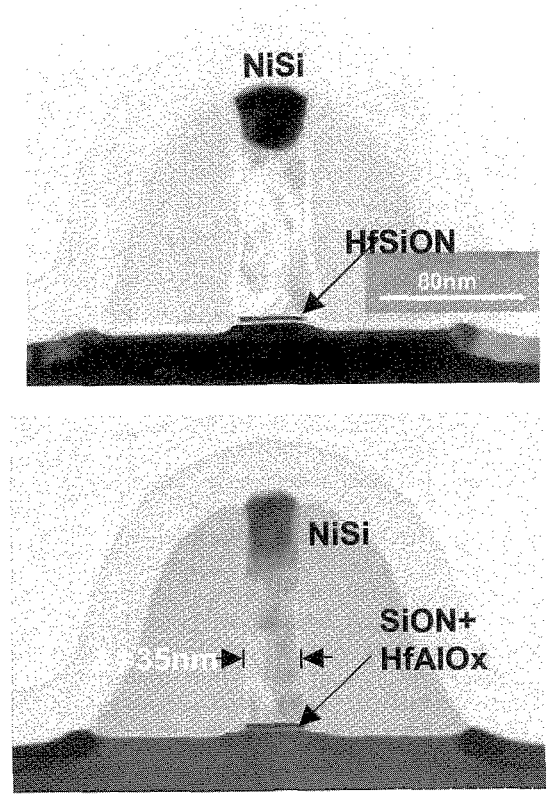

Fig. 1. Cross-sectional TEM photos of fabricated FETs with (a) HfSiON/SiO_2 and (b)HfAlOx/SiON gate insulators [5, 6].

3. RESULTS AND DISCUSSION

3.1 Gate negative stress

Under gate negative stress (n-FET accumulation or p-FET inversion), an abrupt jump in the gate current was observed. Weibull β decreases with the IL thickness, and the TDDB lifetime itself also becomes short with the IL thickness [5, 6].

In order to evaluate the interface degradation by the stress, the charge pumping current was measured with periodic interrupt of constant voltage stress (CVS). As shown in Fig. 3, the number of interface states increases under negative gate stress, while it is much smaller under positive stress. The rate of increase in the number of interface states is almost the same irrespective of high-k materials if they were plotted as functions of the amount of injected charge. These results on TDDB lifetime, Weibull β, and charge pumping indicate that the abrupt jump corresponds to the IL-breakdown (BD).

X-ray photoelectron spectroscopy measurements indicated that the band gap, valence band (VB) offset, and conduction band (CB) offset of the present HfAlOx film with respect to Si(100) were 6.5, 3.6, and 1.78 eV, respectively [8], and those for HfSiON were 6.9, 2.92, and 2.86 eV, respectively [6].

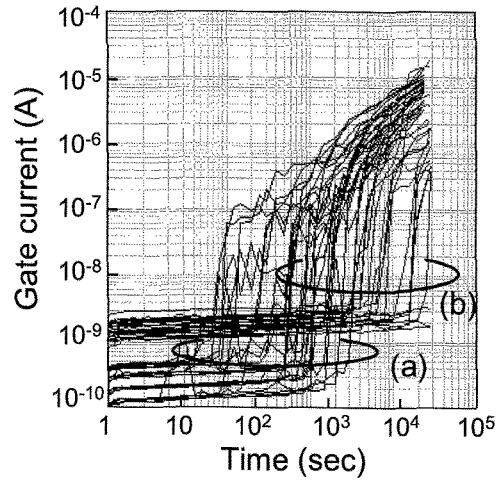

Fig. 2. Time evolutions of gate current in p-FET under gate negative stress. (a) HfAlOx (EOT=1.4nm), (b) HfSiON (EOT=1.55nm).

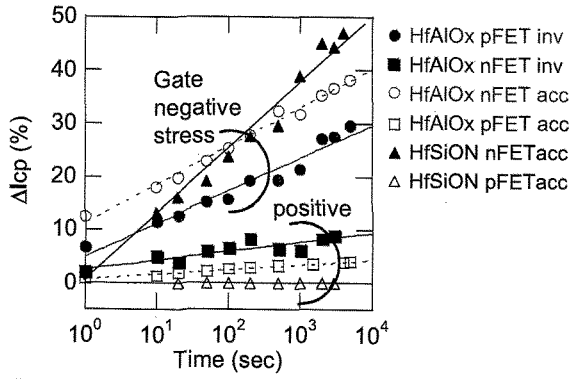

Fig. 3. Interface state generation by constant current stress [7].

Although VB offset is larger than CB offset, carrier separation measurements revealed that holes are the dominant both for HfSiON and HfAlOx [5, 6].

According to charge pumping and carrier separation measurements, we investigated the effect of holes on the interface state generation using first principle calculations. Pseudo-potential calculations on a plane wave basis have been performed within the framework of the generalized gradient approximation (GGA) [9]. Plane waves up to 25 Ry were used for bases. As a model for IL/Si interface, we used the SiO_2/Si interface structure model proposed by Kageshima and Shiraishi [9]. A schematic illustration of the structure is shown in Fig. 4. One oxygen atom was removed and Si dangling bonds were terminated by hydrogen atoms.

The total energies of the HfO_2 and SiO_2/Si system were calculated. With no holes in the HfO_2, the system lose 1.83eV by moving hydrogen from the SiO_2/Si interface to the HfO_2, while a gain of about 1.66eV is obtained when holes are present in HfO_2. This calculation implies that hole injection promotes a chemical reaction in which a hydrogen atom terminating a Si dangling bond is extracted, forming the $(\equiv Hf\text{-}OH\text{-}Hf\equiv)^+$ bond. Thus, it is believed that the hydrogen release from the Si/SiO_2(SiON) interface is the most probable explanation of the IL-BD.

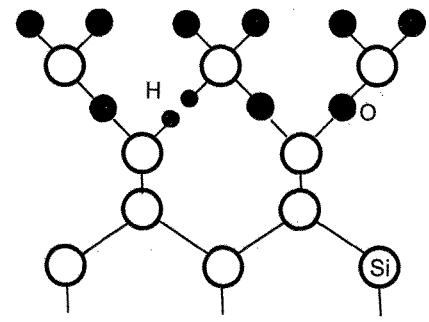

Fig. 4. Schematic illustration of SiO_2/Si interface. The structure proposed by H. Kageshima [1] was used; one oxygen atom was removed and the dangling bonds were terminated by hydrogen atoms [7].

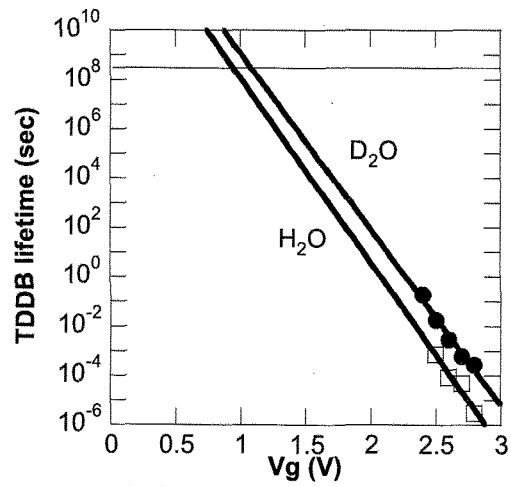

Fig. 5. TDDD lifetimes of HfAlOx/SiON formed by D_2O- and H_2O-ALD.

We can introduce deuterium into the IL by using D_2O instead of H_2O in the ALD process. As shown in Fig. 5, TDDB reliability was improved by deuterium incorporation. This result supports the hydrogen release model for IL-BD.

In order to evaluate electronic defect states in the dielectric stack structure, we measured total photoelectron yields as functions of photon energy in the range from 4.0 to 5.7 eV. The obtained PYS spectrum was shown in Fig. 6(a). As illustrated by this figure, the photon energy is normalized by the signal corresponding to the Si valence electron. From the first derivative of the yield spectrum, the energy distribution of the filled defect state density was crudely estimated. As shown in Fig. 6(b), the defect state densities were as high as 10^{13} cm^{-3} at the silicon valence band edge.

The following model for the hole conduction is proposed based on this result. Under the negative gate bias, electrons leave HfSiON to Si, i.e., holes are injected into HfSiON. An electron from VB of the poly-Si gate would fill the unoccupied electron trap leaving a hole. The hole is extracted by the negative gate bias. As a result, holes flow from the substrate to the gate (see Fig. 7).

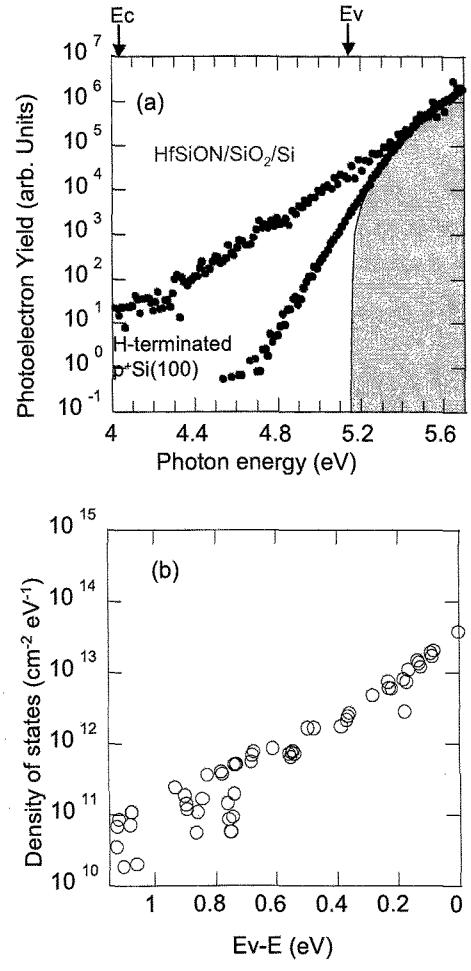

Fig. 6. Photoelectron yield spectra and electron occupied density of state of HfSiON/SiO_2/Si and H-terminated p+Si(100) [7].

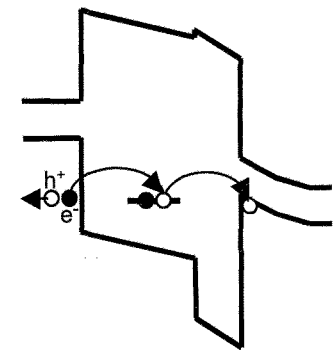

Fig. 7. Schematic explanation for hole conduction in high-k/SiO_2 gate insulators [7].

A.S. Foster *et al.* [10] reported that the energy levels of oxygen interstitial (**Io**, **Io**$^-$, **Io**$^{2-}$) were in the HfO_2 band gap and were lower than Si VBM. Present calculations gave similar results. **Io**$^{2-}$ and **Io**$^-$ generate defect levels at 1 – 1.5 eV above HfO_2 VBM. It is probable that **Io**-related defects, constituting the electron traps detected by the PYS measurements, are responsible for hole conduction.

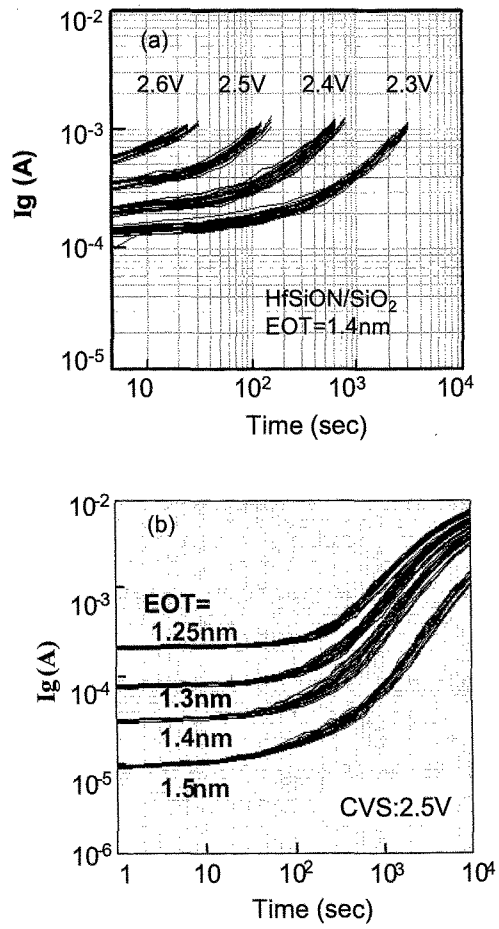

Fig. 8. Time evolutions of gate current in p-FET under gate positive stress. (a) HfSiON, (b) HfAlOx.

3.2 Gate positive stress

Under gate positive stress (n-FET inversion or p-FET accumulation), a gradual increase in the gate leakage as "SILC" was observed instead of an abrupt jump (Fig. 8) [5, 6] .

A good candidate for the trap responsible for SILC in electron current is oxygen vacancy. It is reported that shallow traps exist at around 0.5- 0.8eV below the HfO_2 conduction band minimum (CBM) [11] and it is believed that these traps are related to the oxygen vacancies. H. Takeuchi *et al.* reported that they detected defects at about 1.2eV below CBM of HfO_2 by spectroscopic ellipsometry and they deduced that these defects were oxygen vacancies [12].

We calculated the energy levels of oxygen vacancy using DFT-PBE based molecular dynamics with Δt=0.5 a.u. and μ_e=900 a.u. Periodic 96 atom supercell was used. The obtained values of **Vo** levels are summarized in Table 1. Oxygen defects generate defect levels between Si CBM and HfO_2 CBM.

Table 1. Summary of oxygen vacancy levels measured from HfO_2 CBM obtained by 1st principle calculations.

Temp.	Vo^0	Vo^{2+}	$Vo^0 - Vo^{2+}$
300K	1.73	0.41	1.32 (eV)
1000K	1.91	0.22	1.69 (eV)

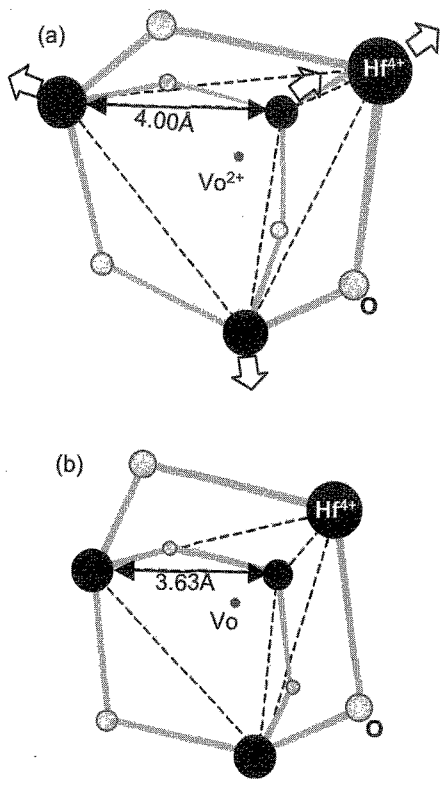

Fig. 9. Typical structure of HfO_2 with oxygen vacancy, (a) with $\mathbf{Vo^{2+}}$, (b) with $\mathbf{Vo^0}$ [7].

It is found that the defect level of $\mathbf{Vo^{2+}}$ shifts downwards by trapping electrons. Taking into account the well-known band gap underestimation in the first principle calculations, the energy shifts due to a electron trapping were estimated to be 1.0 – 1.6 eV. These values are for crystalline HfO_2, and the defect levels would be distributed in amorphous films.

The energy shifts by electron trapping are due to the structural variations. Figure 9(a) shows the structure of HfO_2 with $\mathbf{Vo^{2+}}$. The distance between two Hf atoms is stretched to 4.0Å from 3.63Å and the Hf-O-Hf bond angle is widened to 131° from 109° by removing O^{2-} from HfO_2. By trapping two electrons, these are successively relaxed to 3.65Å and 112°, leading to a lowering of energy level.

These structural variations can be understood as follows: by removing O^{2-}, Hf^{4+} ions move outwards by coulomb repulsion. When electron trapping occurs, coulomb repulsion becomes weak, and Hf ions move back toward the original position.

Based on these results, a possible scenario for the SILC in the electron current is as follows: electrons injected from the substrate tunnel through the IL, and are captured by traps, $\mathbf{Vo^{2+}}$. The defect level shifts downwards by lattice relaxation. Some of the trapped electrons are released to the CBM of gate poly-Si either via HfO_2 CB or tunneling, while some of them are trapped again by another $\mathbf{Vo^{2+}}$ (Fig. 10). The numbers of $\mathbf{Vo^{2+}}$ themselves or that of the electron trapped defects ($\mathbf{Vo^+}$) increases with stress, leading to SILC.

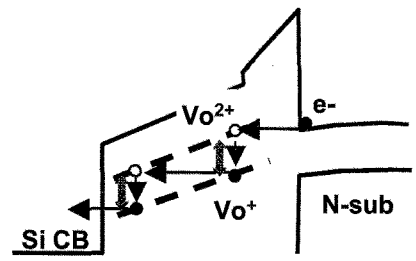

Fig. 10. Schematic explanation for SILC in electron current.

If the electrons hopping between $\mathbf{Vo^{2+}}$ and $\mathbf{Vo^+}$ or electron release from $\mathbf{Vo^+}$ to the HfO_2 conduction band occurs, temperature dependence of the electron current should be observed. As shown in Fig. 11, temperature dependence of the electron current is evident while the hole current exhibits no temperature dependence. Using the trap-assisted tunneling model [13], electron trap level was estimated to be 1.6eV. The good agreement between the theoretical calculation and the experimental data suggests that oxygen vacancies are responsible for the electron current conduction.

Carrier separation measurements using p+gate n-FET indicates that the hole current does not increase initially but commences increasing after a certain period of CVS [6]. The hole current increase can also be explained by the energy shift of $\mathbf{Vo^{2+}}$, as shown in Fig. 12. When the number of $\mathbf{Vo^+}$ increases, valence band electrons also tunnel through these defects, resulting in hole current increase.

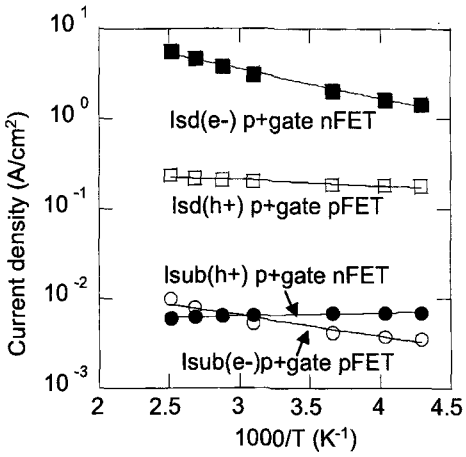

Fig. 11. Temperature dependence of electron and hole current in a p+gate nFET under positive bias (Vg=+2.5V) and a p+gate pFET under negative bias (Vg=-2.5V) [7].

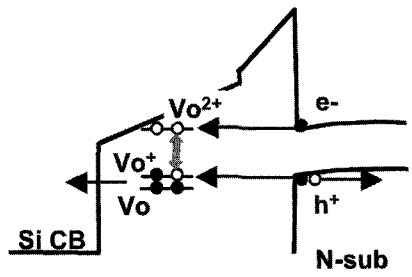

Fig. 12. Variations in the oxygen defect-level structure induced by electron trapping and possible conduction mechanism of hole current [7].

4. CONCLUSIONS

The role of oxygen-related defects on the reliability degradation in HfO_2-based high-k/SiO_2(SiON) gate stacks was studied and possible microscopic models were proposed. A large hole current observed under gate negative bias could be attributed to the electron injection from the gate into the defect level due to oxygen interstitials. Hole-injection was found to stimulate the release of hydrogen from Si-H terminations, causing of IL-BD. Under gate positive stress, SILC in electron current was observed. Oxygen vacancies provide a conduction path for trap-assisted tunneling, which is responsible for the electron current increase. Due to the structural variation, **Vo** level shifts downwards 1 to 1.6eV, leading to an increase in electron current due to valence electron tunneling.

5. REFERENCES

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