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Transient Characteristics of $HfAlO_x$ Gate Dielectric Films

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Transient capacitances and current during application of step voltages to the gate electrode of metal-oxide-semiconductor (MOS) structures with stacked gate dielectrics were investigated. The behaviors of the transient characteristics have been well explained by trapping and detrapping of both negative and positive charges. It was also found that negative charges were trapped near the gate electrodes during stress voltage application, while positive charges were trapped near the Si/SiO_2 interface. The transient characteristics during relaxation revealed the possibility of the charge detrapping as a reason for the transient current.

Key words: high-k dielectrics, MOS, transient capacitance, transient current, trap, detrap

1. INTRODUCTION

High dielectric constant (high-k) materials for use as gate dielectric films in sub-100 nm technology have been widely investigated [1-5]. In particular, there has been interest in the electrical transient characteristics, such as dielectric relaxation current [2-4].

One of the major problems in metal oxide films such as HfO_2, ZrO_2, Al_2O_3 and $BaSrTiO_3$ [5] is formation of charge-trapping centers. It is probably because these films can be formed only by deposition. Even SiO_2 film is known to have a number of charge-trapping centers and interface charges when it is deposited [6]. Thus, it is clear that we should be aware of how much charge trapping and detrapping occurs in a high-k film or an interlayer in device use, especially those that are in a transient state. In particular, charge detrapping can influence the transient characteristics of metal-oxide-semiconductor field effect transistors (MOSFETs) with a high-k gate film [7]. In addition, for such a material with a high density of trapping centers, the transient current observed after decrease of the gate voltage could also be related to charge detrapping together with dielectric relaxation.

In this study, we have investigated transient behaviors during stress voltage application and relaxation of MOS capacitors with hafnium-aluminum binary oxide ($HfAlO_x$) deposited on thermally grown SiO_2 interlayer. The transient characteristics are correlated with charge trapping and detrapping.

2. EXPERIMENT

MOS capacitors were formed on CZ-grown, p-type Si(100) substrates. First, 0.9-nm-thick SiO_2 interlayer was formed on the Si substrates by thermal oxidation. Then, $HfAlO_x$ [Hf/(Hf+Al)=29%] was deposited on the SiO_2 interlayer by atomic layer deposition (ALD), followed by post-deposition annealing (PDA) at 1050°C in O_2/N_2 atmosphere (with an oxygen content of 0.2%) for 1 s. The thickness of the $HfAlO_x$ films was 7 nm. Then, 150 nm thick phosphorus-doped polycrystalline Si (poly-Si) films were deposited on top by low-pressure chemical vapor deposition (LPCVD). For the measurements of the electrical properties, the poly-Si film was patterned by photolithography and etching. The gate areas were 100×100 μm^2.

The electrical properties of the capacitors were characterized by transient phenomena. The initial leakage current-voltage (*I-V*) and capacitance-voltage

(*C-V*) characteristics were investigated. The capacitors were then kept under negative stress gate voltages for 20 min so as to be under the accumulation condition. Both transient leakage currents and transient capacitances were measured during application of the stress gate voltages. The capacitors were then relaxed by a sudden decrease in the gate voltages down to the initial flatband voltage V_{fb}, which was characterized by the initial *C-V* measurement. Charge trapping and detrapping behaviors were investigated by measuring transient capacitance during stress voltage application and relaxation. The signal frequency and voltage during the capacitance measurements were 10 kHz and 30 mV, respectively. The transient current was also measured during relaxation; its relation to charge detrapping is discussed below.

3. RESULTS AND DISCUSSION

A typical *C-V* curve of fresh MOS capacitors is shown in Fig. 1. Fitting the *C-V* characteristics to the calculated curve indicated that the effective oxide thickness was 2.2 nm. The flatband voltage was also estimated as -0.53 V. By taking into account ideal flatband voltage, it was found that the capacitors initially had negative charges. This is similar to the Al_2O_3 film in a previous study [8].

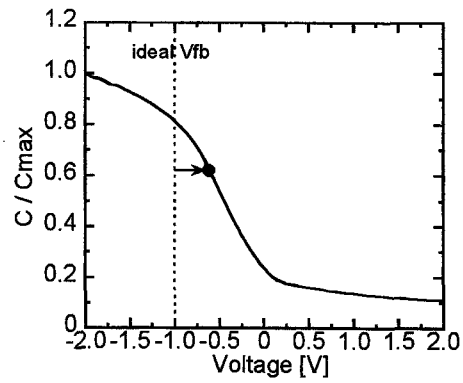

Fig. 1. An initial capacitance-voltage curve.

Figure 2 shows transient capacitances during application of stress gate voltage. The applied voltages were varied from -1.0 to -3.0 V. The capacitance values were normalized with the value obtained at 1 s. It can be seen that the capacitance decreased for all stress voltages. This capacitance reduction corresponds to the negative shift of the *C-V* curve, which results from the positive charge trapping and/or the negative charge detrapping. These two phenomena cannot be distinguished by the electrical measurements. However, only charge trapping should be considered, which occurs by current flow during stress application, since the initial state before stress application is in thermal equilibrium. That is, the capacitance reduction denotes that the positive charges were trapped in the stacked gate dielectrics.

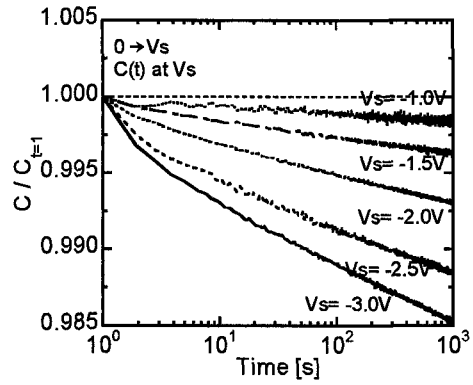

Fig. 2. Transient capacitances during application of stress gate voltages. The stress voltages are varied from -1.0 to -3.0 V.

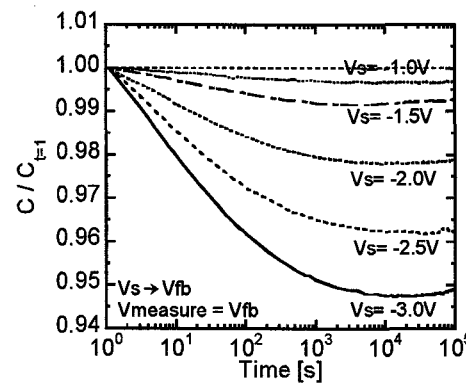

Fig. 3. Transient capacitances during relaxation after decreasing various gate voltages to the initial flatband voltage, -0.53 V.

Next, we discuss the transient capacitance during relaxation. Figure 3 shows the transient capacitances during relaxation after steeply decreasing the stress gate voltage (V_S) to the initial flatband voltage, -0.53 V. The stress voltages were varied from -1.0 to -3.0 V. The gate voltage was kept at -0.53 V while measuring the capacitances. This figure shows that within 10^4 s the capacitances decreased with lapse of time for all stress voltages, corresponding to the negative shift in the *C-V* curves. It is quite reasonable to consider that during

relaxation, these capacitance reductions are closely related to charge detrapping. The capacitance reduction, however, can only be explained by negative charge detrapping, which is inconsistent with the fact that positive charges were trapped during stress application, as quoted above. Detrapping of positive charges was seen only after relaxation for 10^4 s as a capacitance increment.

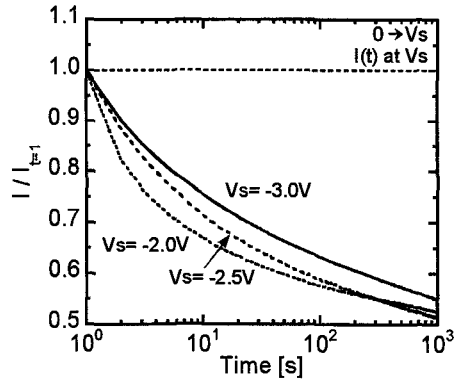

Fig. 4. Transient currents during application of stress gate voltages. The stress voltages are -2.0, -2.5 and -3.0 V.

To decipher the discrepancy, the transient leakage currents were measured during stress voltage application. Figure 4 shows the measured transient currents, where the stress voltages were -2.0, -2.5, and -3.0 V. It is obvious that the current reduced with lapse of time for all stress voltages. Since for $HfAlO_x$ film, the energy barrier height for electrons at the interface with the cathode is lower than that for holes at the interface with the anode [9], electrons are considered a main contributor to the current flow. The current reductions can be attributed to the increment of the barrier height due to electron trapping near the gate electrodes.

By taking into account the transient capacitances and currents, a qualitative model for the trapped charges in the $HfAlO_x$ films is proposed in Fig. 5. During stress application, when $V = V_S$, negative charges are trapped relatively near the gate electrode, while positive charges are trapped relatively near the Si/SiO_2 interface. It has been reported that Si atoms can reach the film surface because of the reaction between the high-k metal oxide and the Si substrate during deposition of the metal oxide [10, 11]. The Si atoms possibly cause the surface layer to have a high concentration of negative charge-trapping centers. The negative charges trapped far from the Si substrate weakly contribute to Si band bending, while the positive charges trapped near the Si/SiO_2 interface strongly affect Si band bending. This is why positive charge trapping was only observable in transient capacitance measurements.

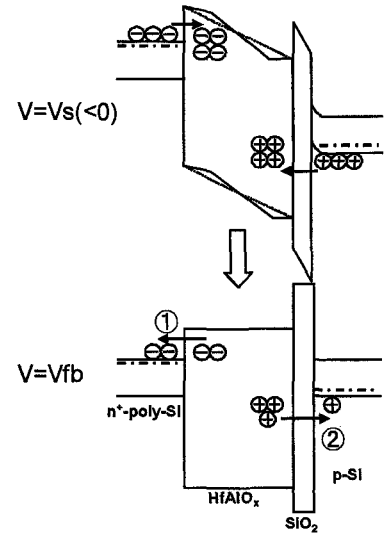

Fig. 5. A qualitative model of trapped charge distribution after stressing.

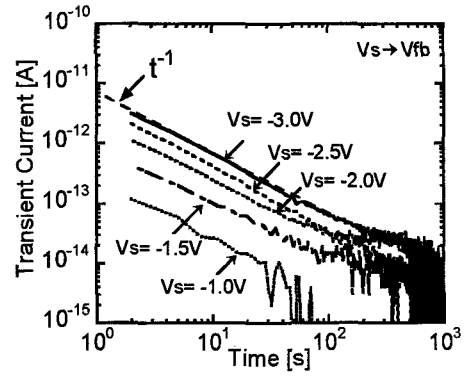

Fig. 6. Transient currents during relaxation after decreasing the gate voltages to an initial flatband voltage of -0.53 V. The stress gate voltages are varied between -1.0 and -3.0 V.

In relaxation, these trapped charges are detrapped. From the transient capacitance measurement shown in Fig. 3, it is concluded that relaxation occurs first by negative charge detrapping, followed by a positive charge release.

The transient phenomenon can also be viewed as a transient current. Figure 6 shows the transient current obtained after reduction of the stress voltages down to the initial flat band voltage, -0.53 V. The stress voltages

were varied from -1.0 to -3.0 V. The figure clearly reveals the transient behavior with time by t^{-1} for all stress voltages. This characteristic has been reported as the current due to dielectric relaxation, where rearrangement of dipole moment in dielectric film occurs by alteration of the external field [2-4]. Our present results, however, indicate the necessity to take into consideration the charge detrapping after the voltage reduction.

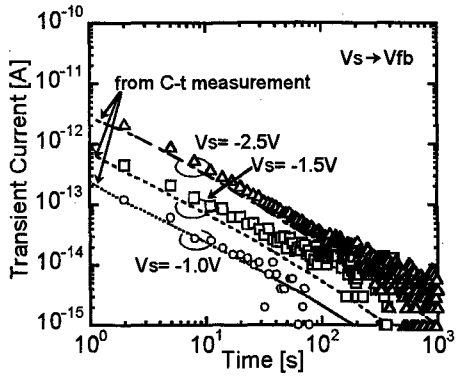

Fig. 7. Transient currents during relaxation after decreasing stress gate voltage to initial flatband voltage. The dashed lines are calculated currents from capacitance discharge.

A discussion of the influence of the charge detrapping on the transient current follows. Under a constant applied voltage, the discharge current of a capacitor, J_{dc} is expressed as,

$$J_{dc}(t) = C_g \frac{dV_g(t)}{dt} \quad (1)$$

with C_g and V_g being the capacitance of the stacked dielectric film and the voltage applied across the film, respectively. Figure 7 again shows the transient current during relaxation. The stress voltages were -1.0, -1.5, and -2.5 V. The dashed lines represent the calculated currents from eq. (1). The voltage alterations across the dielectric film were obtained from the amounts of *C-V* curve shifts, estimated from the transient capacitance measurement. Apparently, the measured transient currents are thoroughly explained by the capacitance discharge in this figure. The discharge can be easily attributed to a release of the trapped negative charge, as described above. Although the dielectric relaxation should not be dismissed, it suggests the possibility that the transient current observed in the present dielectric film results from the charge detrapping.

4. SUMMARY

The transient capacitances of the MOS capacitors with stacked gate dielectrics were investigated. We can see that negative charges were trapped near the gate electrodes, while the positive charges were trapped near the Si/SiO_2 interface during stressing. Detrapping proceeds much faster for the negative charges than positive charges. The transient current measurements revealed the current is proportional to t^{-1} during relaxation. From the perspective on the capacitance discharge, the detrapping behavior was found to be possible reason to lead to the transient current.

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