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Electrical Characterization of HfAlOx/SiON Dielectric Gate Capacitors

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We analyzed the charge-trapping properties, soft breakdown field, and time-dependent dielectric breakdown (TDDB) characteristics of HfAlOx(3-7nm, Hf/(Hf+Al)=~0.3)/SiON(1.2nm) stack gate dielectrics on p-Si(100). During constant voltage stress with negative gate voltages, the leakage current through the dielectric is gradually decreased by electron trapping until soft breakdown occurs, irrespective of the HfAlOx thickness. Concurrently, negative flat-band voltage shift presumably due to anode hole injection is increased with voltage stress for capacitors with 7nm-thick and 5nm-thick HfAlOx, and the increment of net positive charges is reduced with a decrease in the HfAlOx thickness. For the case with 3nm-thick HfAlOx, the negative flat-band voltage shift is reduced by voltage stress. These results can be interpreted in terms that electron trapping near the gate side and hole trapping near the substrate interface occur during the voltage stress. An enhancement of the electric field near the interface between HfAOx and SiON due to the above-mentioned charge trapping and the recombination of electrons and holes at the HfAOx/SiON interface may play a role in the breakdown mechanism. Considering that in soft breakdown, the average electric fields in HfAlOx and in SiON were estimated to be 3-4 and 10-13MV/cm, respectively, it is likely that the soft breakdown is triggered by the degradation near the HfAlOx/SiON interface.
Key words: HfAlOx/SiON, Charge trapping, Soft-breakdown field, TDDB

1. INTRODUCTION

Continuous scaling of metal-oxide-semiconductor (MOS) field-effect transistors (FETs) requires high-k gate dielectric as a replacement for conventional silicon oxide gate dielectric to suppress the gate leakage current at an allowable level. From the viewpoints of favorable energy-band alignment with Si(100) and gate materials [1, 2] and of good thermal stability [3], Hf-based silicates or aluminates have been most intensively evaluated as alternative gate dielectrics, and their scalability to SiO_2 equivalent thickness below 1nm has often been discussed while arguing on some of their drawbacks, such as mobility degradation and undesirable threshold voltage shift [4]. To minimize such drawbacks, the control of the top and bottom interfacial layers is of great importance. Another major concern for the implementation of high-k dielectric stack is dielectric reliability. Recently, it was reported that for FETs with HfAlOx(Hf/(Hf+Al)=~0.3)/SiON dielectric stacks, the hole-current from the substrate is higher than the electron current from the gate electrode in n-FET accumulation or p-FET inversion [5], and for the n^+-poly gate pFET with HfAlOx(Hf/(Hf+Al)=~0.6)/SiO_2 dielectric layers, the dominant carrier in the gate leakage current changes from electron to hole when interface layer (IL) thickness is thinner than ~2.0nm [6]. The behavior of hole and electron trapping in the stack dielectric induced by leakage current is of great importance to understand the breakdown mechanism, and the reliability of metal-gate/high-k gate stack still needs to be researched.

In this paper, we focus on the reliability of capacitors consisting of Al gate and HfAlOx(Hf/(Hf+Al)=~0.3)/SiON stacks on p-Si(100). The soft breakdown mechanism is discussed based on charge trapping characteristics and TDDB characteristics at room temperature.

2. EXPERIMENTAL

The substrates used in this work were p-type Si(100) wafers with a resistivity of ~10Ω·cm. After standard wet-cleaning steps of the wafers, a 1.2nm-thick oxynitride interfacial layer (IL) was formed by a process sequence of NH_3 annealing at 700°C and subsequent oxidation at 850°C in NO ambient. The HfAlOx(Hf/(Hf+Al)=~0.3) films in the thickness range of 3-7 nm were deposited on IL by an atomic layer chemical vapor deposition (ALCVD) method, in which trimethy-aluminum, tetrakis ethyl- methylamino hafnium, and water were used as precursors, and NH_3-plasma treatment was performed at each cycle of ALCVD. The post-deposition anneal was carried out at 1000°C for 1s in 0.2% O_2 diluted by N_2. Finally, Al gates with a diameter of 0.5mm were formed on top.

3. RESULTS AND DISCUSSION

3.1 Charge trapping characteristics

In order to investigate the charge trapping effects in the HfAlOx/SiON gate stacks, current-voltage (I-V) measurement with a gate voltage sweep rate of 20mV/s and capacitance-voltage (C-V) measurements at conditions of 1kHz and 5mV/s were carried out before and after constant voltage stress (CVS) at room

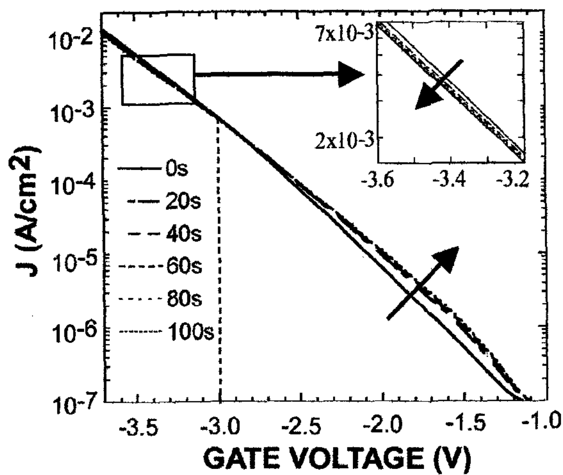

Fig. 1. The gate leakage current as a function of gate voltage before and after constant voltage stress at –3.8V for MOS capacitor with 3nm-thick HfAlOx.

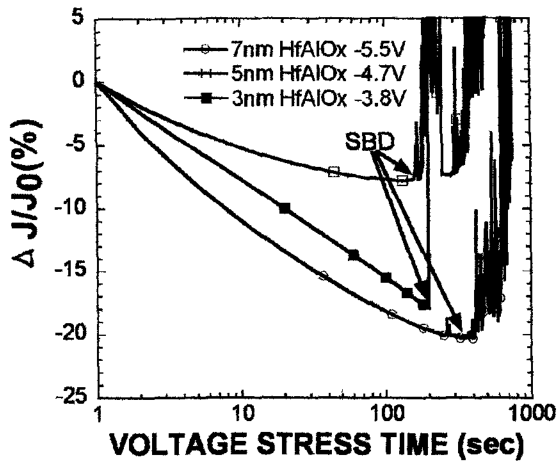

Fig. 2. Time dependence of the current density during CVS at 3.8MV/cm in HfAlOx for MOS capacitors with different HfAlOx thicknesses.

temperature. Figure 1 shows the gate leakage current measured for the capacitor with 3nm-thick HfAlOx at a stress voltage of –3.8V corresponding to an average electric field of 3.8M/V in HfAlOx, where the cumulative stress time is a parameter. At negative gate voltages lower than –3V, the gate leakage current was increased with stress time, which is analogous to the stress-induced leakage current (SILC) in silicon oxide and associated with the trap assisted tunneling process [7]. In contrast, at negative gate voltages higher than -3V, the leakage current tends to be decreased with progressive stress. As shown in Fig. 2, a distinct decrease in the leakage current during CVS is observable until soft breakdown occurs at an average electric field of ~3.8MV/cm in HfAlOx independent of the HfAlOx thickness, and is attributable to the defect generation and electron trapping at generated defects. Figure 3 shows changes in C-V curves for capacitors with 7nm-thick and 3nm-thick HfAlOx with CVS. For the case with 7nm-thick $HfAlO_x$, the C-V curve shifts toward the negative gate voltage side with progressive stress at –5.5V (~3.8MV/cm), which indicates an increase in net positive

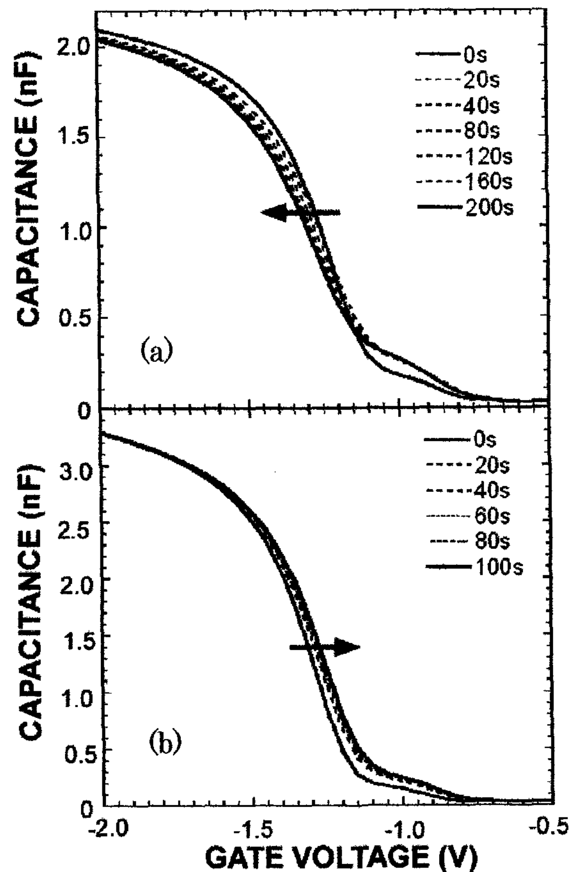

Fig. 3. The C-V curves (1KHz) before and after CVS for capacitors (a) with 7nm-thick HfAlOx stressed at –5.5V and (b) with 3nm-thick HfAlOx stressed at –3.8V.

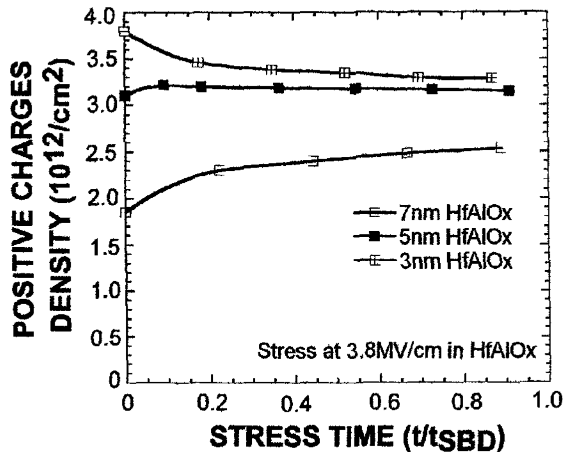

Fig. 4. Change of positive charges density as a function of stress time normalized by soft breakdown time for capacitors with different HfAlOx thicknesses.

charges possibly caused by anode hole injection. On the other hand, for the case with 3nm-thick $HfAlO_x$, negative charges were generated during CVS; namely, net positive charges are reduced as evaluated from the flat-band voltage shift from the ideal C-V curve. No significant change in the C-V hysteresis is observed for all the cases. In Fig. 4, the temporal changes in the effective net positive charges with CVS at 3.8MV/cm in HfAlOx are summarized as a function of the stress time normalized

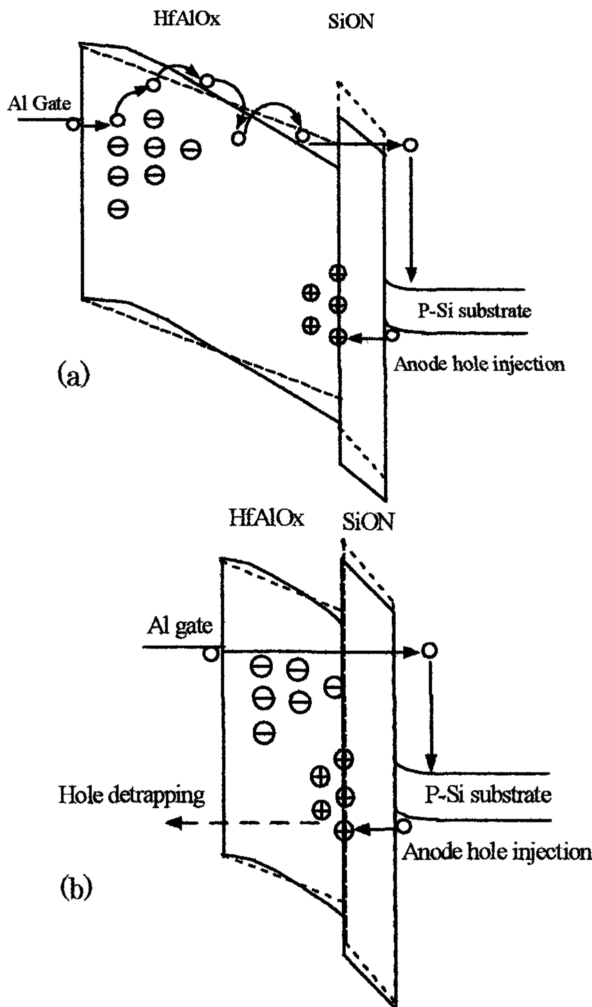

Fig. 5. Energy band diagram with charge trapping at CVS ~3.8MV/cm for capacitors (a) with 7nm-thick HfAlOx and (b) with 3nm-thickHfAlOx.

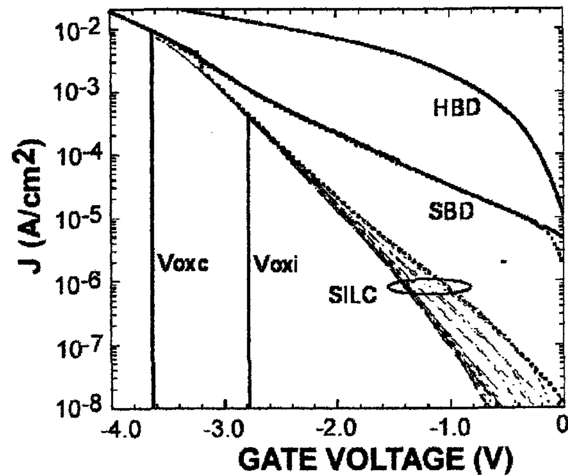

Fig. 6. The leakage current as a function of oxide voltage for the capacitance with 5nm-thick $HfAlO_x$.

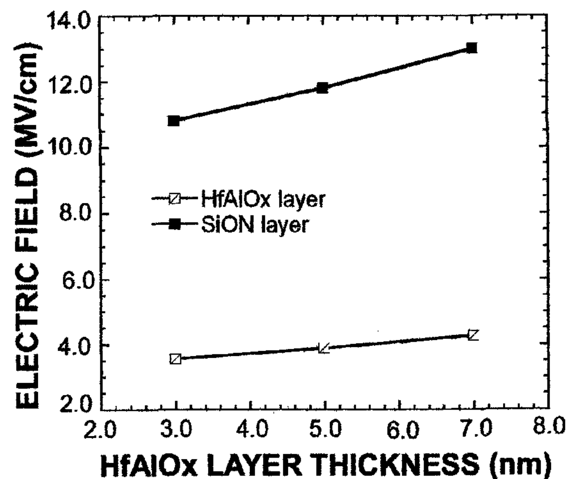

Fig. 7. Electric fields in HfAlOx and SiON as function of $HfAlO_x$ layer thickness when SBD occurs.

with time to soft breakdown t_{SBD}. For the capacitor with 7nm-thick HfAlOx, the account of effective net-positive charges was increased from 1.8 $x10^{12}/cm^2$ with stress time and tends to be saturated around $2.5x10^{12}/cm^2$. For the capacitor with 5nm-thick HfAlOx, little increase in the effective net-positive charges with stress was observable, and the effective net-positive charges were decreased from $3.8x10^{12}/cm^2$ to almost the same level as the saturated effective net-positive charges for the case with 3nm-thick HfAlOx. In the initial stage before stress, the decrease in the effective net positive charge with increasing HfAlOx layer thickness implies that net negative charges exist in the HfAlOx layer, presumably due to electron trapping, and positive charges near the HfAlOx/SiON interface and/or in the SiON interfacial layer. Since the influence of the charges in the gate dielectric on the flat-band voltage is increased with the product of the net charge density at a certain distance from the gate and the distance between the sheet charge and the gate, it is likely that the defect generation during CVS results in electron trapping in HfAlOx near the gate side and hole trapping near HfAlOx/SiON interface and/or in the SiON interfacial layer.

Considering the conduction mechanism for the cases with 5nm-thick and 7nm-thick is dominated by Frenkel-Poole emission and for the case with 3nm-thick HfAlOx by direct tunneling [8], energy band diagrams for the cases with 7nm-thick and 3nm-thick HfAlOx were drawn with and without trapped electrons and holes (Fig. 5). For simplicity, in Fig. 5, the charge distribution in the dielectric prior to CVS is ignored. For the case with 7nm-thick HfAlOx (Fig. 5 (a)), one or two shallow traps involving Frenkel-Poole emission exist in the thickness direction. By electron trapping in HfAlOx near the gate and hole trapping near the HfAlOx/SiON interface, the energy band diagram is modified for the electron injection to be suppressed and for the electric field near the HfAlOx/SiON interface to be enhanced. The trapped holes far from the gate cause the negative flat-band voltage shift. For thinner HfAlOx, the net sheet charge can be reduced (Fig. 5 (b)) and a decrease in the positive charge due to the neutralization of trapped holes with injected electrons and hole detrapping may occur.

3.2 Critical electrical field to soft breakdown

In order to evaluate an oxide electric field critical to

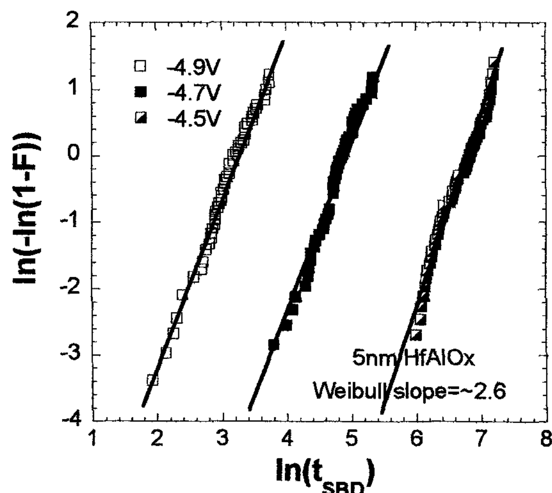

Fig. 8. Time to SBD Weibull distribution at different voltage stresses with 5nm-thick HfAlOx.

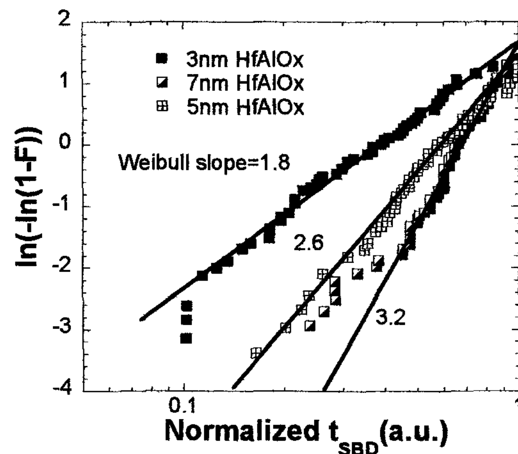

Fig. 9. Time to SBD Weibull distribution of HfAlOx/SiON stacks dielectric with different HfAlOx thicknesses, where the time to SBD was normalized by its maximum.

soft breakdown, the gate voltage was ramped up and down at a rate of 20mV/sec to a maximum value, which was increased by a 20mV step for each cycle of voltage scan. Figure 6 shows the measured current versus the oxide voltage for a capacitor with 5nm-thick HfAlOx, where the oxide voltage is obtained by subtracting the flat band voltage and the surface potential of the accumulation layer. A dielectric degradation quite similar to ultra-thin silicon oxide [9] is observed. With an increase in the maximum negative oxide voltage from V_{oxi}, the leakage current is gradually increased as seen in the SILC of SiO_2 until a dramatic increase in the leakage current is observed at the maximum oxide voltage of V_{oxc}. We defined V_{oxc} as the soft breakdown voltage. The soft breakdown voltage for each of the capacitors with different $HfAlO_x$ thicknesses was determined from Weibull plots at 63% failures. At SBD, the average electric fields for 3nm-thick and 7nm-thick HfAlOx are estimated to be 3.5 and 4.3MV/cm, respectively. Correspondingly it is found that the electric field in SiON is increased from 10.8 to 13 MV/cm with increasing physical thickness. The estimated electric field in HfAlOx is less than two thirds of the theoretically predicted breakdown field according to the experimental function $E_{BD}=24.5(\kappa)^{-0.51}$, where κ is dielectric constant [10]. For capacitors with thinner HfAlOx, increased current density at CVS may be responsible for decreased electric field critical to soft breakdown. Based on the energy band diagrams shown in Fig. 5, the enhanced electric field near the HfAlOx/SiON interface and the electron and hole recombination near the interface may play a role in the dielectric degradation during ramp voltage stress.

3.3 TDDB characteristics

The time to soft breakdown was defined as the stress time when the first sudden increase or fluctuation of gate current occurs. Weibull distributions of TDDB were measured at different stress voltages as represented in Fig. 8. Obviously, the constant Weibull slope, for example ~2.6 for capacitors with 5nm-thick HfAlOx, can be determined irrespective of the stress voltage. The Weibull distributions for capacitors with different HfAlOx thicknesses are shown in Fig. 9, where the time to SBD was normalized by its maximum. The Weibull slope is increased with HfAlOx thickness as seen in ultrathin SiO_2 [9] and the obtained values are comparable to the reported ones for SiO_2 with the same EOT.

4. CONCLUSIONS

Al-gate capacitors with HfAlOx/SiON stack gate dielectrics were evaluated by I-V and C-V measurements. During constant voltage stressing under negative bias polarity, the electron trapping in HfAlOx near the gate and the hole trapping proceed near the HfAlOx/SiON interface. The enhancement of the electric field near the HfAlOx/SiON interface due to such charge trapping may trigger the soft breakdown. The slope of Weibull plots for TDDB characteristics was evaluated to be 1.8 or higher, being comparable to the case of ultrathin-SiO_2.

5. ACKNOWLEDGMENTS

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6. REFERENCES

[1] J. Robertson, J. Vac. Sci. Technol. B13 (2000) 1785.
[2] S. Miyazaki, J. Vac. Sci. Technol. B19 (2001) 2212.
[3] M. Kundu et al., Appl. Phys. Lett. 86 (2004) 5326.
[4] M. Gardner et al., *Int. Workshop on Gate Insulator, (Tokyo, 2003) p. 170.*
[5] K.Torii et al., *IEEE Int. Electron Devices Meeting, (San Francisco, 2004) p.129.*
[6] W. Mizubayashi et al., Appl. Phys. Let. 85 (2004) to be published.
[7] Z. Xu et al, J. Appl. Phys. 91 (2002) 10127.
[8] S. Nagamachi et al., *Abst. of 15th Symp of Mat. Res. Soc. of Japan (Tokyo, 2004) p.128.*
[9] W. Mizubayashi and S. Miyazaki, Jpn. J. App. Phys, 43 (2004) 6925.
[10] J. McPherson et al., Appl. Phys. Lett. 82 (2003) 2121.

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