

Fabrication of Polycrystalline Si Thin Film Transistor using Plasma Jet Crystallization Technique

H. Kaku, S. Higashi, S. Miyazaki, M. Asami*, H. Watakabe*,
N. Andoh* and T. Sameshima*

Grad. School of AdSM, Hiroshima Univ., Kagamiyama 1-3-1, Higashi-Hiroshima

Fax: 81-82-422-7038, e-mail: semicon@hiroshima-u.ac.jp

* Tokyo Univ. of A&T, Nakamachi 2-24-16 Koganei

Fabrication of polycrystalline Si thin-film-transistors using a plasma jet crystallization technique (PJC) has been studied. Hydrogenated amorphous Si (a-Si:H) films are crystallized with the power input to the plasma source of 1.6-2.6 kW and substrate scanning speed of 170-1000 mm/sec. Thin film transistors (TFTs) fabricated using the crystallized films showed good electrical characteristics. By increasing input power from 1.86 to 2.29 kW in the crystallization, the average field-effect mobility was increased from 42 to 61 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, and the threshold voltage was decreased from 4.0 to 3.4 V. These results indicate that the PJC technique is a very promising low-temperature process technology.

Key words: thermal plasma jet, crystallization, polycrystalline Si, thin-film transistor

1. INTRODUCTION

For the fabrication of large area electronic devices such as solar cells and thin-film transistors (TFTs), the crystallization of Si films on glass substrates at low temperatures is one of the key process technologies. So far, the applications of Ar ion laser [1-3], excimer laser [4,5] and solid state laser [6] to the film crystallization have been studied extensively. These techniques can make good crystallinity Si films with low thermal damage to substrates by melting and crystallizing Si films within a short period of ns to μs . However, due to a limit on the output laser power, the application of the laser crystallization techniques to large area processing leads to difficulties for reduction in the process cost. Therefore, the development of a crystallization technique with high power and a simple equipment structure as a replacement of the laser crystallization has been strongly required.

Recently, we reported a crystallization technique of Si films on glass substrates using thermal plasma jet [7] in which high power density of several tens of kW/cm^2 is achieved at atmospheric pressure with a simple equipment structure. In this work, we extended our research to demonstrate the feasibility of this technique for the crystallization of Si films on the glass substrate and the application of the plasma jet crystallization (PJC) technique to TFT fabrication.

2. EXPERIMENTAL

A thermal plasma source was developed as shown in the inset of Fig. 1. The W cathode and the water-cooled Cu anode separated 2 mm each other was connected to a power supply. Arc discharge was performed by supplying DC biases of 13 - 15.3 V and 130 - 200 A between the electrodes with an Ar gas flow of 3 to 8 L/min. The thermal plasma jet was formed by blowing out the arc plasma through an orifice of 4 mm in diameter. Hydrogenated amorphous Si films in the thickness range of 80 - 910 nm were formed on quartz substrate from an inductively coupled plasma (ICP) of 50% SiH_4 diluted with H_2 at 150°C . The substrate was linearly moved by a motion stage in front of the plasma jet with scanning speed ranging from 170 to 1000 mm/s. The distance between the plasma source and the substrate was set at 2 mm. The crystalline qualities of the films were evaluated by Raman scattering and ultra-violet (UV) reflectivity measurements. A 441.6 nm line from a He-Cd laser was used as an excitation light for Raman scattering. The surface morphology of the films was observed by atomic force microscopy (AFM).

TFTs were fabricated by the following process. $7 \times 10^{20} \text{ cm}^{-3}$ -phosphorus-doped a-Si films with a thickness of 25 nm were deposited by plasma-enhanced chemical vapor deposition (PECVD) on quartz substrates and then patterned into islands to form source and drain regions. 20-nm-thick intrinsic a-Si films were deposited on the source/

drain islands by PECVD of 50% SiH₄ diluted with H₂ at 150°C. The PJC was performed to crystallize the a-Si film and to activate the phosphorus atoms in source and drain regions, simultaneously. The intrinsic layer thickness was set at 20 nm to allow the diffusion of the impurities in the underlying doped Si film to the top intrinsic layer and the formation of good ohmic contacts with Al electrodes. In the PJC, at a constant scanning speed of 700 mm/s, the power input to the plasma source was varied from 1.86 to 2.29 kW. After etching the Si layer to an island shape, source and drain contacts were formed by the evaporation of Al, followed by the deposition of a 100-nm-thick gate SiO_x film by molecular beam deposition from SiO powder in an oxygen radical atmosphere at room temperature [8].

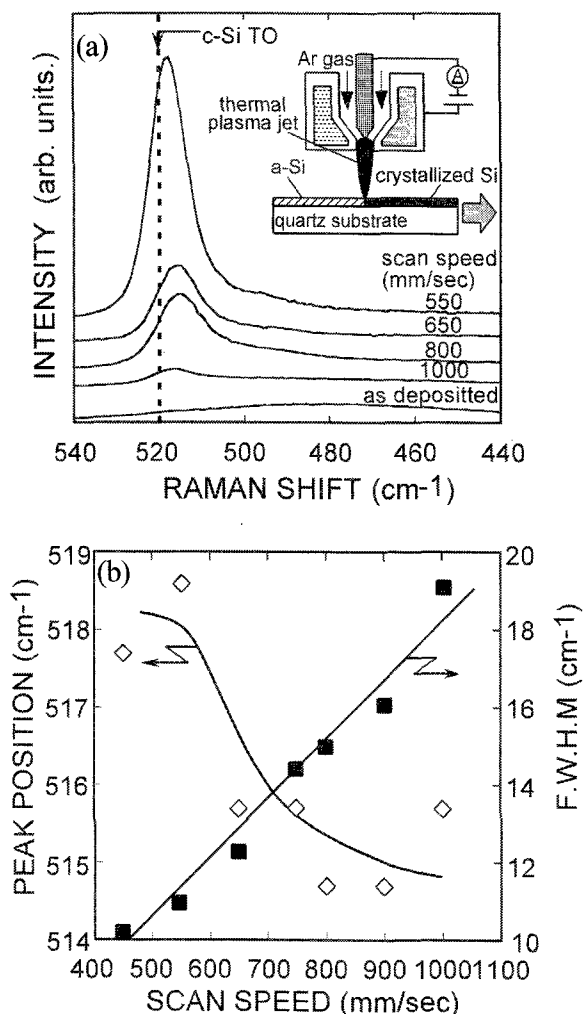


Fig. 1. Raman scattering spectra obtained from as-deposited and plasma-jet-treated Si films with the constant power input to the plasma source of 2.4 kW and different scan speeds ranging from 550 to 1000 mm/s (a) and the full width at half maximum (FWHM) and position of crystalline Si TO phonon peaks (b) as a function of scan speed.

After the gate electrode formation by Al evaporation, high-pressure H₂O vapor annealing was performed at 260°C, and 1.3×10^6 Pa for 3 h to reduce defect states in the Si film and at the gate SiO_x/Si interface [9, 10]. The maximum temperature throughout the fabrication process was 260°C.

3. RESULTS AND DISCUSSION

Figure 1 (a) shows the Raman spectra of 80 nm-thick Si films before and after anneal at different scanning speeds under a constant input power to the plasma source of ~ 2.4 kW. By reducing the scanning speed below 1000 mm/s, a sharp peak due to crystalline Si TO phonons appears in the range from 515 to 518 cm⁻¹. This confirms that Si films are crystallized by the thermal plasma jet. With decreasing scanning speed from 1000 to 450 mm/s, the full width at half maximum (FWHM) is reduced from 19 to 10 cm⁻¹ and the peak position of the TO phonon band is increased from 515 to 518, respectively, as shown in Fig. 1(b). These results indicate that the crystalline quality of the Si films is improved by decreasing the scanning speed. Amorphous Si films can be crystallized in solid phase and, higher temperature and longer annealing duration have improved the crystalline quality. The amount of glass substrate (OA-10) deformation after the annealing evaluated by a Taly step (DEKTAK) was about 42 nm at most, which indicates no critical change in surface flatness.

Figure 2 shows the crystallization conditions of the input power to the plasma source and the scanning speed. When increasing input power, a-Si films are crystallized at higher scanning speed and the process window becomes larger. This means that the throughput of this crystallization tech-

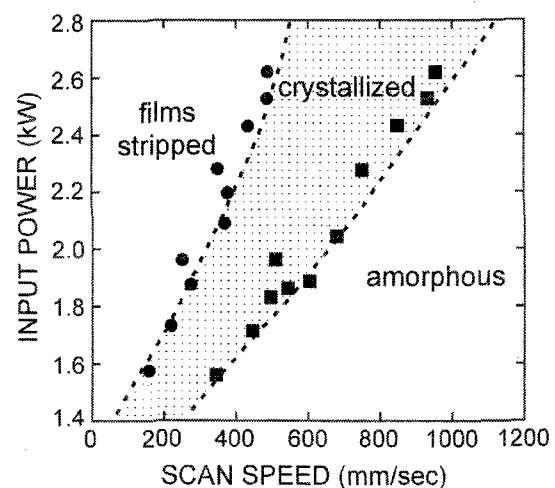


Fig. 2. Crystallization conditions of a-Si films with respect to the power input to the plasma source and the scanning speed.

nique is improved by an increase in the input power to the plasma source. However, the film stripping was facilitated with a decrease in the scanning speed down to a certain value.

We have confirmed a-Si:H films as thick as 1 μm are crystallized by PJC [7]. Figure 3 shows AFM images of 80 nm-thick and 910-nm-thick Si films crystallized by thermal plasma jet with 2.4 kW input power and 1000 mm/sec scanning speed. The surface roughness (root-mean-square value) of the films and the average grain size are 1.7-1.8 nm and 25-26 nm, respectively. This result suggests that the crystallization is governed by the homogeneous nucleation in the a-Si:H film, independent of the film thickness.

The fabricated TFTs show good performance as seen in transfer and output characteristics shown in Figs. 4(a) and (b), respectively. The on-current increases as the power input to the plasma source during the crystallization increases from 1.86 to 2.29 kW as shown in Fig. 4 (a). The field-effect mobility and threshold voltage of the TFTs extracted from the transfer characteristic are shown in Fig.

5. The average field-effect mobility increases from 42 to 61 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ and the threshold voltage decreases from 4.0 to 3.4 V with increasing input power from 1.86 to 2.29 kW. These results agree well with an improvement of crystallinity by the increase in the power input to the plasma source. Namely, the crystalline network with fewer defects is likely to be formed in higher temperature crystallization. From these results, we confirm that the PJC technique is applicable to the fabrication of TFTs.

4. CONCLUSIONS

Amorphous Si films on glass substrate were crystallized by thermal plasma jet under conditions of input power to the plasma source from 1.6 to 2.6 kW and scanning speed of the substrate from 170 to 1000 mm/s. The crystallinity is improved by annealing the films at higher temperature for longer duration. Si films with thickness ranging from 80 to 910 nm were crystallized and the crystallinity of the surface showed little dependence on the thickness. TFTs fabricated using the PJC technique showed an average field-effect mobility that increased from 42 to 61 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ and

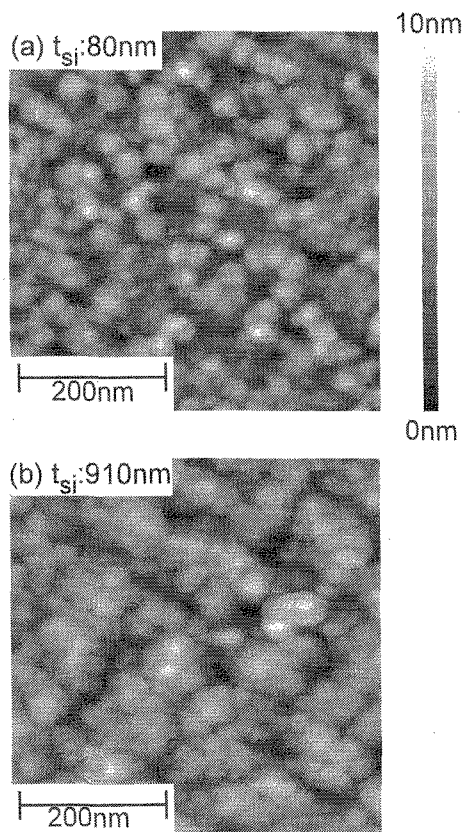


Fig. 3. AFM image of 80 and 910 nm thick Si films crystallized at a input power of 2.5kW and a scanning speed of 1000mm/sec .

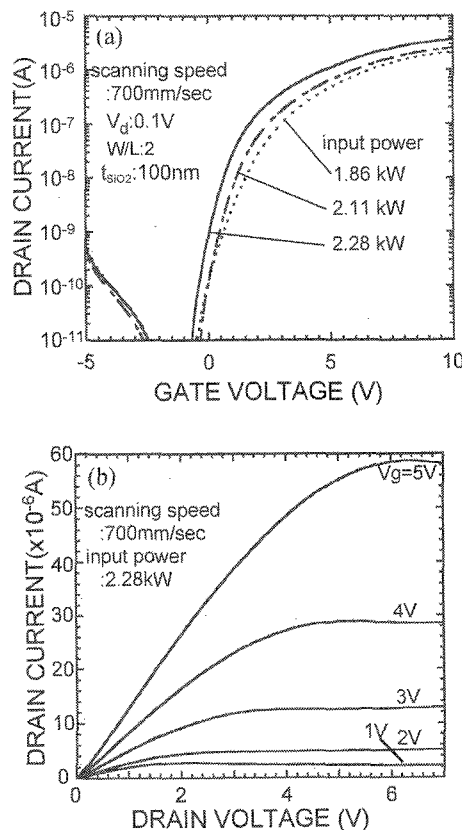


Fig. 4. Transfer (a) and output (b) characteristics of TFTs fabricated by the PJC technique.

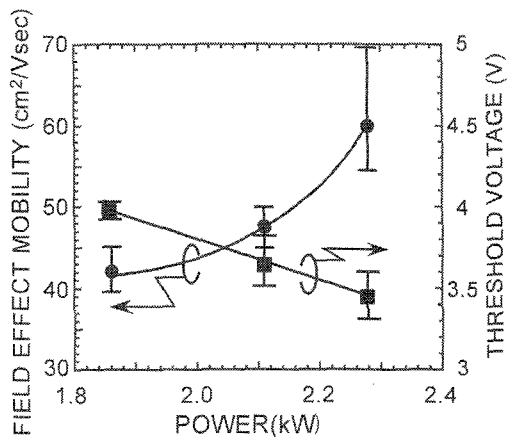


Fig. 5. Average field-effect mobility and threshold voltage extracted from the transfer characteristics shown in Fig. 4(a) as a function of input power. The error bars indicate the maximum and minimum values obtained from three to eight transistors.

a threshold voltage that decreased from 4.0 to 3.4 V with increasing power input to the plasma source during the crystallization from 1.86 to 2.29 kW. These results indicate that the PJC technique is very promising as a low temperature process technology.

REFERENCES

- [1] A. Gat, L. Gerzberg, J. F. Gibbons, T. J. Magee, J. Peng and J. D. Hong, *Appl. Phys. Lett.* 33 775 (1978).
- [2] R. A. Lemons, M. A. Bosch, A. H. Dayem, J. K. Grogan and P. M. Mankiewich, *Appl. Phys. Lett.* 40 469 (1982).
- [3] A. Doi, T. Asakawa and S. Namba, *Jpn. J. Appl. Phys.* 28 L128 (1989).
- [4] T. Sameshima et. al., *IEEE Electron Device Lett.* EDL-7, 276 (1986).
- [5] S. Higashi and T. Sameshima, *Jpn. J. Appl. Phys.* 40 480 (2001).
- [6] A. Hara, F. Takeuchi, M. Takei, K. Suga, K. Yoshino, M. Chida, Y. Sano and N. Sasaki: *Jpn. J. Appl. Phys.* 41 L311 (2002).
- [7] H. Kaku, S. Higashi, H. Taniguchi, H. Murakami and S. Miyazaki, *Appl. Surf. Sci.* (2004) to be published.
- [8] H. Watakabe and T. Sameshima, *IEEE Trans. Electron devices* 49 2217 (2002).
- [9] T. Sameshima and M. Satoh, *Jpn. J. Appl. Phys.* 36 L 687 (1997).
- [10] T. Sameshima, M. Satoh, K. Sakamoto, K. Ozaki and K. Saitoh, *Jpn. J. Appl. Phys.* 37 L 1030 (1998).