Transactions of the Materials Research Society of Japan 31[1] 77-80 (2006)

Ferroelectric and Structural Properties of $Bi_4Ti_3O_{12}$ Thin Films with TiO_2 Layer Prepared on $Ir/Ti/SiO_2/Si$ Substrates

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$Bi_4Ti_3O_{12}$ (BIT) thin films with TiO_2 anatase buffer layer were deposited on the $Ir/Ti/SiO_2/Si$ substrates by metalorganic chemical vapor deposition using $Bi(CH_3)_3$ and $Ti(i\text{-}OC_3H_7)_4$ sources. The BIT thin film with TiO_2 buffer layer exhibited highly *a*- and *b*-axes-oriented BIT single phase. The as-deposited BIT thin film with TiO_2 buffer layer exhibited the ferroelectricity without postannealing. The ferroelectricity depends on the flow rates of $Ti(i\text{-}OC_3H_7)_4$ and $Bi(CH_3)_3$ source. When the flow rates of Ti and Bi were fixed at 90 and 20 sccm, respectively, the as-deposited BIT thin film with TiO_2 buffer layer on $Ir/Ti/SiO_2/Si$ substrate exhibited a good *P-E* hysteresis loop.

Key words: $Bi_4Ti_3O_{12}$ (BIT) thin film, MOCVD, TiO_2 anatase buffer layer, $Ir/Ti/SiO_2/Si$ substrate

1. INTRODUCTION

Ferroelectric $Bi_4Ti_3O_{12}$ (BIT) has a spontaneous polarization in the *a-c* plane at an angle approximately 4.5° with the *a*-axis, and exhibits two independently reversible components along the *c*- and *a*-axes [1-4]. It shows coercive fields (E_c) of 3.5 kV/cm and 50 kV/cm, and remanent polarization (P_r) values of 4.0 and 50 μC/cm^2, and dielectric constants of 160 and 130 along the *c*-and *a*-axes, respectively. The BIT thin films are expected for application to nonvolatile ferroelectric memory (NV-FeRAM) devices with nondestructive readout operation. Therefore, BIT thin films have been prepared by several deposition techniques such as sol-gel [5-7], metalorganic chemical vapor deposition (MOCVD) [8-25], metalorganic decomposition (MOD) [26,27], and RF magnetron sputtering [28-32]. However, it is difficult to prepare the perfect undoped BIT thin film. This is because interdiffusion occurs between the electrode and the poly-Si-plug during ferroelectric film formation at high temperature.

In recent years, Nakamura *et al.* has prepared the BIT thin films with a TiO_2 anatase buffer layer on the $Pt/Ti/SiO_2/Si$ substrates by MOCVD [22-25]. The BIT thin film with the TiO_2 anatase buffer layer prepared at 500°C exhibited highly *a*- and *b*-axes-oriented BIT single phases, although the BIT thin film with no buffer layer exhibited a *c*-axis orientation. The interface between the BIT thin film and the substrate was very smooth. The BIT thin film consisted of small grains and exhibited a good *P-E* hysteresis loop. The ferroelectricity of the BIT thin film with the TiO_2 anatase buffer layer strongly depends on the thickness ratio of the BIT thin film to the TiO_2 anatase layer, indicating that the TiO_2 anatase buffer layer acts not as barrier layer but as an initial nucleation layer of the BIT thin film. When the thickness ratio is fixed at $[(BIT)/(TiO_2)]=15$, the remanent polarization (P_r) and the coercive field (E_c) were $2Pr=81.6$ μC/cm^2 and $2E_c=250$ kV/cm, respectively. The dielectric constant (ε_r) was 160. The above results originate to the effect of TiO_2 buffer layer [25]. Such an effect is also expected for BIT thin film on $Ir/Ti/SiO_2/Si$ substrate.

In this study, we have prepared the undoped BIT thin films with TiO_2 anatase buffer layer on the $(111)Ir/Ti/SiO_2/Si$ substrates by MOCVD. MOCVD is the most promising practical preparation method because it enables realization of high thickness and composition uniformity over large film areas. TiO_2 layer can be prepared at a low substrate temperature of 350°C by MOCVD using a $Ti(i\text{-}OCH_3H_7)_4$ source [24,25]. Therefore, we believe that the TiO_2 anatase buffer layer is very effective for low-temperature fabrication below 500°C and for inducing interdiffusion between the BIT thin film and the Ir substrate. In this paper, we present the structural and ferroelectric properties of the BIT thin films with a TiO_2 buffer layer and discuss about the mechanism of TiO_2 buffer layer.

2. EXPERIMENTAL

The TiO_2 Anatase buffer layers were prepared on $(111)Ir/Ti/SiO_2/Si$ substrates by MOCVD. Tetra-isoproxy titanium[$Ti(i\text{-}OCH_3H_7)_4$], which was supplied by TRI Chemical Laboratory Inc., was used as the Ti source of MOCVD. The pressure in the reaction chamber was fixed at approximately 5 Torr. The $Ti(i\text{-}OCH_3H_7)_4$ vaporized in a separate stainless-steel babbler was maintained at 40°C. The substrate temperature (Ts) was approximately 350°C.

BIT thin films were deposited on the TiO_2 anatase buffer layer prepared on $Ir/Ti/SiO_2/Si$ substrates by MOCVD using an apparatus having a vertical cold-wall-type reaction chamber. Trimethyl bismuth $[Bi(CH_3)_3]$ and $Ti(i\text{-}OCH_3H_7)_4$, which were supplied by TRI Chemical Laboratory Inc., were used as Bi and Ti sources of MOCVD. The $Bi(CH_3)_3$ and $Ti(i\text{-}OCH_3H_7)_4$, vaporized in separate stainless-steel bubblers were maintained at 0°C and 40°C, respectively. The Ar and O_2 gases were used as the carrier gas and the oxidizing gas, respectively. The pressure in the reaction chamber was fixed at approximately 5 Torr. The Ts was fabricated at 500°C in all BIT thin films. The total thickness of the BIT thin film and buffer layer was fixed at 400 nm. Finally, the top Pt electrodes with a diameter of 0.2 nm were deposited on the film surface through a metal shadow mask by RF-magnetron sputtering in order to measure electrical properties.

The structural properties of the BIT thin films were characterized by X-ray diffraction (XRD) using CuKα. The surface morphology and cross section were observed by atomic force microscopy (AFM). The electrical properties were measured using the feroelectric property measurement system RT-6000HVS manufactured by Radiant Technologies Inc. The polarization-electric field (*P-E*) hysteresis loop were measured using one-shot triangular waveforms with a period of 50 ms.

3. RESULTS AND DISCUSSION

Figure 1 shows the XRD pattern of the as-deposited TiO_2 anatase thin film prepared at Ts=350°C. The film thickness of the TiO_2 buffer layer was approximately 50nm. A broad peak at 2θ=28.4 ° is the Si(111)peak. A weak peak at 2θ=25.3 ° is (101) peak of TiO_2 anatase. In recent years, TiO_2 anatase thin film has been prepared on $Pt/Ti/SiO_2/Si$ substrate by MOCVD [24]. The orientation of TiO_2 anatase on $Pt/Ti/SiO_2/Si$ substrate is different from that of TiO_2 anatase on $Ir/Ti/SiO_2/Si$ substrate, although the preparation conditions such as Ti source, flow rates of Ar gas and O_2 gas and Ts are same in both TiO_2 thin films. This is considered to originate to the lattice mismatch between TiO_2 anatase and substrate.

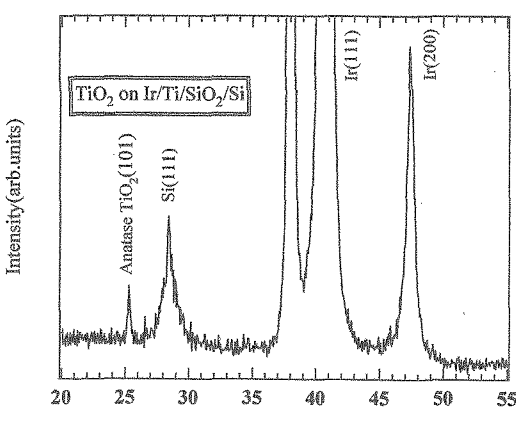

Fig.1 XRD pattern of TiO_2 anatase thin film prepared on $Ir/Ti/SiO_2/Si$ substrate.

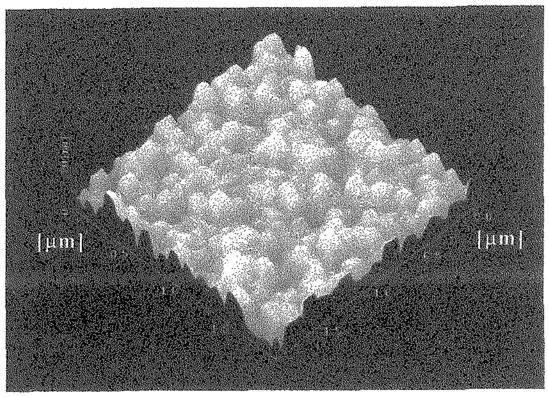

Fig.2: AFM image of TiO_2 anatase thin film prepared on $Ir/Ti/SiO_2/Si$ substrate.

Figure 2 shows the AFM image of TiO_2 anatase thin film prepared on $Ir/Ti/SiO_2/Si$ substrate. The thin film consist of small grain of 50~100 nm. The surface roughness is 20 nm against the film thickness of 50 nm.

Figure 3 shows the XRD pattern as a function of the Ti flow rate in the as-deposited BIT thin films with the TiO_2 anatase buffer layer. The Bi flow rate was fixed at 20 sccm. The Ts was ~500°C. The thicknesses of BIT and TiO_2 anatase thin films were 350 nm and 50 nm, respectively. The BIT thin films prepared at the Ti flow rates of 60 sccm and 75 sccm exhibit the existences of excess Bi and pyroclore phases at 2θ~28.0°. On the other hand, the BIT thin films prepared at the Ti flow rates of 90 sccm and 96 sccm exhibit highly *a*- and *b*-axes oriented BIT single phase. The *a*- and *b*-axes orientation increases with increasing Ti flow rate.

Figure 4 shows the composition ratios of Bi and Ti as a function of the Ti flow rate in the as-deposited BIT thin films with the TiO_2 anatase buffer layer. When the Ti flow rates are 60 and 75 sccm, the BIT thin films are Bi-excess and Ti-poor. However, the composition ratios of Bi and Ti are almost stoichiometric composition in Ti flow rates of 90 sccm and 96 sccm. These results accord with the XRD patterns of Fig. 3.

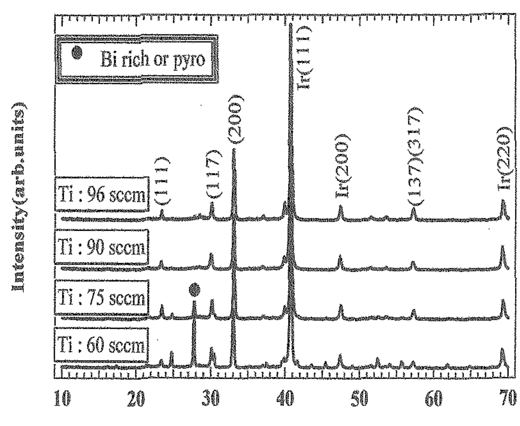

Fig.3 XRD patterns of BIT thin film with TiO_2 anatase buffer layer as a function of Ti flow rate. The Bi flow rate was fixed at 20sccm.

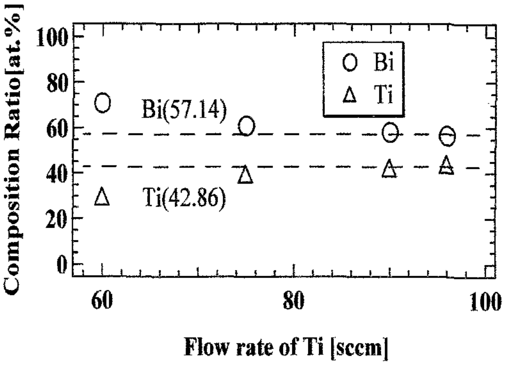

Fig.4: Compositions of Bi and Ti of BIT thin film with TiO_2 anatase buffer layer as a function of Ti flow rate. The Bi flow rate was fixed at 20 sccm.

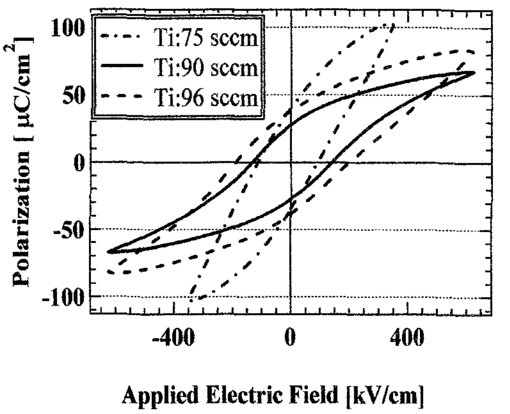

Fig. 5: Hysteresis loops of as-deposited BIT thin films with TiO_2 anatase buffer layer as a function of Ti flow rate. Bi flow rate was fixed at 20sccm.

Figure 5 shows *P-E* hysteresis loops a function of the Ti flow rate in the as-deposited BIT thin films with the TiO_2 anatase buffer layer. The BIT thin film with TiO_2 buffer layer prepared at the Ti flow rate of 60 sccm did not exhibit the *P-E* hysteresis loops. This is due to the existences of excess Bi and pyroclore phases. The BIT thin films prepared at the Ti flow rate above 70 sccm exhibited the *P-E* hysteresi loops. When the flow rate is 70 sccm, the hysteresis is unique fat shape. The shape of hysteresis loop is improved in the Ti flow rate of 90 sccm. Then, the *Pr* and *Ec* are $2P_r$=55.9 μC/cm^2 and $2E_c$=259 kV/cm, respectively. The thin film consist of small grain of 50~100 nm. The surface roughness is 20 nm against the film thickness of 50 nm.

The above results are not enough for application of ferroelectric nonvolatile memories, which have stacked capacitor cell structures. However, the interdiffusion between the BIT thin film and the substrate is controlled in BIT thin film with TiO_2 buffer layer on Ir/Ti/SiO_2/Si substrate. This is because the Ti flow rate of the BIT thin film is higher than that of BIT thin film on Pt/Ti/SiO_2/Si substrate [24]. To further investigate the electrical properties of the BIT thin films on Ir/Ti/SiO_2/Si substrate, it is necessary to perform a more systematic optimizations of the film thickness of TiO_2 anatase buffer layer and T_s.

4. CONCLUSION

We have prepared the BIT thin film with the TiO_2 anatase buffer layer on Ir/Ti/SiO_2/Si substrate by MOCVD technique. The orientation depends on the Ti flow rate. When the Ti flow rate is fixed at 90 sccm, The as-deposited BIT thin films with the TiO_2 anatase buffer layer crystallized at 500°C exhibited highly *a*- and *b*-axes orientation. Then, the P_r and E_c of the BIT thin films with TiO_2 anatase buffer layer were $2P_r$=55.9 μC/cm^2 and $2E_c$=259 kV/cm, respectively. Finally, we would like to propose that TiO_2 anatase is a promising buffer layer for low-temperature crystallization of BIT thin films.

ACKNOWLEDGEMENT

This work was supported by a Grant-In- Aid for Scientific Research from the Ministry of Education, Culture, Sports, Science and Technology.

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(Received December 10, 2005; Accepted January 31, 2006)