Transactions of the Materials Research Society of Japan 31[1] 133-136 (2006)

Fabrication of Multiply-Stacked Si Quantum Dots for Floating Gate MOS Devices

K. Makihara, M. Ikeda, T. Nagai, H. Murakami, S. Higashi and S. Miyazaki
Graduate School of Advanced Sciences of Matter, Hiroshima University
Kagamiyama 1-4-1, Higashi-Hiroshima 739-8530, Japan
TEL:+81-82-424-7648, FAX:+81-82-422-7038
E-mail: semicon@hiroshima-u.ac.jp

Abstract

Multiply-stacked structures, in which Si quantum dots (Si-QDs) of ~$6x10^{11}$ cm^{-2} in areal number density and of ~4 nm in average dot height were stacked between ultrathin SiO_2 interlayers, were fabricated by repeating a dry process sequence consisting of remote plasma pretreatments of the SiO_2 surface, Si dot formation by low pressure chemical vapor deposition (LPCVD) using SiH_4 and surface oxidation by a remote O_2 plasma. Cross-sectional transmission electron microscope (TEM) images of so-prepared samples confirm successful fabrication of multiply-stacked Si-QDs in SiO_2 as designed. For Al-gate metal-oxide-semiconductor (MOS) capacitors with 6-stacked Si-QDs in SiO_2, unique hysteresis characteristics were observed by capacitance–voltage (C-V) and displacement current-voltage (I-V) measurements, and attributed to electron charging to and discharging from the Si-QDs as a floating gate because of their independence of the frequency in the range from 100Hz to 1MHz. Also, in the cases that electrons were locally injected into or extracted from multiply-stacked Si-QDs using a conductive probe of an atomic force microscope (AFM) and resultant surface potential changes were measured by a non-contact AFM Kelvin probe, temporal decay in the surface potential change after each of electron injection and extraction suggests spreading of injected charges in multiply-stacked Si-QDs.
Key words: Si dots, stacked structure, remote plasma treatment, LPCVD, electron charging, floating gate, KFM

1. INTRODUCTION

Silicon nanocrystals embedded in SiO_2 networks have attracted a great deal of interest as quantum dots with discrete charged states and their application to the floating gate of metal-oxide-semiconductor (MOS) memories [1 - 3]. In the floating gate application of Si quantum dots (Si-QDs), there is a requirement to fabricate Si-QDs with an areal number density of the order of ~$10^{12}cm^{-2}$, being comparable to the channel electron concentration, on ultrathin gate oxide in order to modify or control the channel conductance. Other issues which must be taken into concern are related to uniformity in dot size. In our previous work, we demonstrated the self-assembling formation of Si-QDs on ultrathin SiO_2 layers by controlling the early stages of low-pressure chemical vapor deposition (LPCVD) using a SiH_4 gas [4]. Also, we reported that the SiO_2 surface treatment with a dilute HF solution just prior to Si dot formation is quite effective to achieve a uniform size distribution and areal dot density as high as ~$5x10^{11}cm^{-2}$ because Si-OH bonds created on the SiO_2 surface act as reactive sites to precursors such as SiH_2 during LPCVD. In addition, by spatially controlling OH termination of the SiO_2 surface before LPCVD, the selective growth of Si dots has been demonstrated [5]. Thus, in fabricating multiply-stacked structures of Si dots in SiO_2, it is practically crucial to create Si-OH bonds on the SiO_2 surface by a dry process matching with subsequent LPCVD. In that regard, we have recently demonstrated that exposing the SiO_2 surface to a remote Ar plasma and subsequently a remote H_2 plasma leads to efficient creation of OH bonds on the SiO_2 surface as in the case of a dilute HF pre-treatment [4] and consequently to the formation of Si dots as high as ~$1x10^{11}$ cm^{-2} [6].

In this work, we extended our research to fabricate multiply-stacked structures consisting of Si-QDs and ultrathin SiO_2 interlayers through all-dry process steps, in which the Si dot formation by SiH_4-LPCVD, the surface oxidation of Si dots by a remote O_2 plasma and the OH termination of the oxidized surface by remote Ar/H_2 plasma were alternately repeated. We also studied electron charging and discharging from multiply-stacked Si-QDs acting as a floating gate in MOS capacitors and examined progressive spreading of injected charge in the multiply-stacked Si-QDs by an atomic force microscopy (AFM)/Kelvin probe method.

2. EXPERIMENTAL

The substrate used in this work was n-type Si(100) with a donor concentration of ~$1x10^{17}$ cm^{-3}. After conventional wet-chemical cleaning steps of n-Si(100), a 4 nm-thick SiO_2 layer was grown on pre-cleaned Si(100) at 1000°C in dry O_2. The SiO_2 surface was then exposed to pure Ar remote plasma and subsequently to pure H_2 remote plasma at 560°C for 1min in each plasma treatment. The remote plasma was generated in a quartz tube of 10 cm in diameter by inductive coupling with an external single-turn antenna connected to a 60 MHz generator through a matching circuit. The sample was placed on the susceptor at a distance of 32 cm away from the antenna to eliminate ion damage. The VHF power and the gas pressure for the remote Ar plasma pretreatment were maintained at 100 W and 0.1 Torr, respectively, and for the remote H_2 plasma treatment at 200 W and 0.2 Torr, respectively. After the series of remote plasma treatments (the H_2/Ar remote plasma treatments), the formation of Si-QDs was carried out on

plasma-treated SiO_2 in the same reaction chamber at 560°C by LPCVD using pure monosilane under 0.5 Torr. Subsequently, the surface oxidation of Si-QDs was performed at the same temperature by a remote VHF plasma of 1% O_2 diluted with He generated at 50 W and 0.1Torr. For the fabrication of the stacked structures of Si-QDs, the above-mentioned process steps of remote Ar/H_2 plasma treatments, LPCVD and remote plasma oxidation were repeated at 560°C. In the floating gate application, to form a 7.5nm-thick control oxide conformally on the dot layer, an amorphous Si layer was grown on formed Si-QDs by LPCVD of 10% Si_2H_6 diluted with He at 440°C, then the a-Si layer was fully oxidized in dry O_2 at 1000°C. Finally, Al gates of 1mm in diameter for MOS capacitors were formed by a thermal evaporation method through a hard stencil mask.

The changes in surface chemical bonding features and in surface microroughness with the H_2/Ar remote plasma treatments were measured by x-ray photoelectron spectroscopy (XPS) using a monochromatized AlKα radiation and AFM, respectively. To evaluate the dot size distribution and the areal dot density, AFM images were taken in ambient of clean room air. Also, to characterize a multiple-stacked structure fabricated with repetition of the process cycle composing of remote plasma treatments and the Si-QDs formation, cross-sectional observations was carried out using a transmission electron microscope (TEM). The capacitance-voltage (C-V) characteristics of MOS capacitors with a floating gate consisting of 6 stacked Si-QDs were measured at a frequency ranging from 100Hz to 1MHz with a gate voltage sweep rate of 33mV/s at room temperature. The displacement current-voltage (I-V) characteristics were also examined at each step of 10mV after a delay time of 10mV. In addition, to examine the charged states of multiply-stacked Si-QDs caused by electron charging to and discharging from Si-QDs and to evaluate their temporal decay characteristics, topographic and surface potential images were simultaneously taken in repeating fashion by employing a non-contact KFM mode [6] in clean room air.

3. RESULTS AND DISCUSSION

XPS spectra of thermally grown SiO_2/Si(100) before and after the H_2/Ar remote plasma treatments confirm no decrease in the SiO_2 thickness and no increase in surface contaminants while they show a change in the SiO_2 surface to OH termination by the plasma treatments [7]. In addition, no increase in the surface microroughness by the plasma treatments was detectable by AFM images. Figure 1 shows AFM images taken after Si dot formation on thermally grown SiO_2 with and without the plasma pre-treatments. Obviously, by the H_2/Ar remote plasma treatment of thermally grown SiO_2 surface prior to LPCVD, the areal dot density is markedly increased to ~6×10^{11} cm^{-2} which is two orders of magnitude larger than that obtained on the as-grown SiO_2 surface. Also, the size uniformity is significantly improved by the remote plasma treatments, with the result that the full width at the half maximum (FWHM) of the Si-QDs size distribution obtained on plasma pre-treated SiO_2 was reduced by 68% of the value on as-grown SiO_2. Considering that in Si dot formation on the thermally grown SiO_2 surface treated by the remote H_2 plasma without the Ar plasma pretreatment, a dot density of ~7×10^{10} cm^{-2} at most is obtained [7], weakened bonds and dangling bonds created by Ar plasma exposure react efficiently with radicals, ions and excited molecules generated in H_2 plasma. Consequently, a number of OH bonds are generated as nucleation sites during LPCVD.

Figure 2 represents AFM images taken before and after exposing Si dots to the remote O_2 plasma for 10 min. As HF-last n-Si(100) was exposed to the remote O_2 plasma under the same condition, 2.4nm-thick SiO_2 was formed uniformly. The surface morphology of the sample Si dots remains almost unchanged by the remote O_2 plasma oxidation, implying uniform surface oxidation of Si dots as well as HF-last flat Si(100) surfaces. Based on these results as shown in Figs. 1 and 2, we fabricated stacked structures of Si dots embedded in SiO_2 by repeating a process sequence of remote plasma oxidation, H_2/Ar remote plasma treatment and LPCVD, and evaluated the dot size distribution for the cases with different numbers of the Si dot formation as shown in Fig. 3. Obviously, for the 3-9 stacked cases, almost the same distribution in dot height was obtained, which indicates that the Si dot formation was repeated in a well-reproducible fashion. In fact, the fabrication of the stacked structure as expected was confirmed by cross-sectional TEM observations after 10 cycles of Si dot formation and remote plasma treatments as shown in Fig. 4. In the high-resolution images as seen in Fig. 4 (b), we found that lattice images of Si nanocrystallites with a size of ~ 5 nm were stacked accompanied with

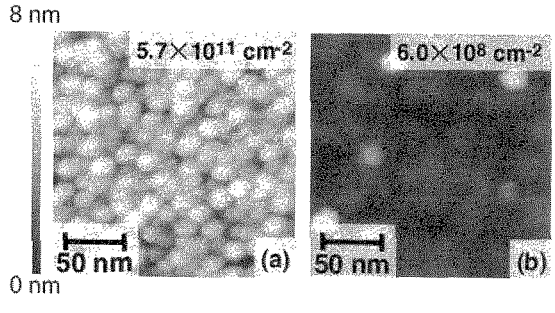

Fig. 1. AFM images taken after Si dot formation on thermal SiO_2 pretreated by H_2/Ar remote plasmas (a) and as-grown thermal SiO_2 (b).

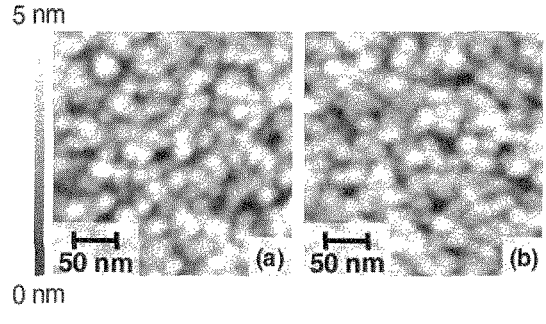

Fig. 2. AFM images of Si dots taken before (a) and after (b) surface oxidation by a remote plasma of 1%O_2 diluted He. The oxide thickness was estimated to be ~2nm.

SiO_2 interlayers.

To asses the usefulness of the series of remote plasma treatments from the viewpoint of the device application, we fabricated Al-gate MOS capacitors with 6 stacked Si-QDs embedded in the gate oxide as a floating gate and evaluated C-V and I-V characteristics (Fig. 5). The C-V curve measured from +3 to -3V is almost identical to the ideal C-V curve for the uncharged floating gate. When the gate voltage is swept over ~0.7 V and backward from the accumulation, a unique hysteresis with a flat-band voltage shift of ~0.24V from the corresponding ideal curve is observed. No change in the hysteresis characteristics was observed in the

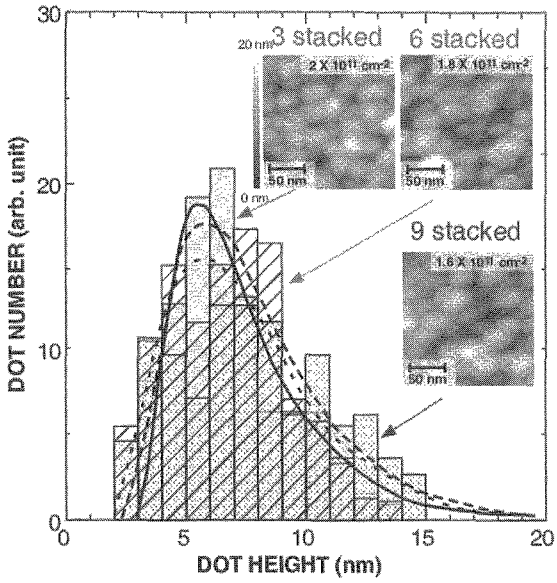

Fig. 3. The dot size distributions evaluated from AMF images for multiply-stacked structures. The corresponding curves denote the log-normal functions well-fitted to the measured size distribution [8].

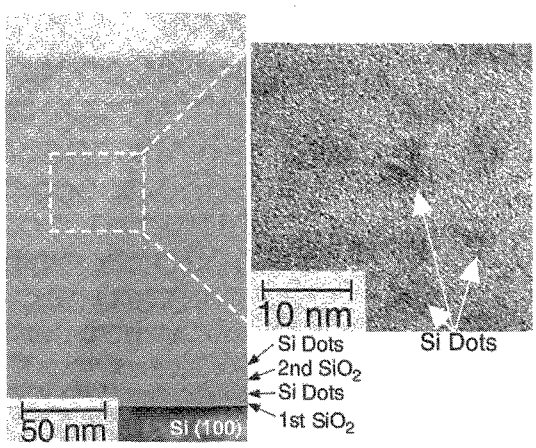

Fig. 4. Cross-sectional TEM images for a stacked structure prepared with 10 cycles of Si dot formation and remote plasma treatments.

frequency range from 100Hz and 1MHz. The capacitance peak measured around the flat-band voltage can be attributed to electron injection into the Si-QDs floating gate from the substrate as seen in the fairly sharp positive peak of the displacement current curve. The discharging current was also measured in the voltage scan backward from the accumulation condition. Notice that the basic features in measured C-V and I-V characteristics are quite similar to those measured for the Si-QDs floating gate MOS capacitors prepared by repeating the sequence of a wet-chemical treatment of the SiO_2 surface using a dilute HF solution, thermal oxidation of Si dot surface and the Si dot formation by LPCVD [9]. The results indicate that the dots act as electric memory nodes as discussed in the cases fabricated without using such plasma pre-treatment, notably without any plasma-induced damages.

To get an insight into the progress on the charge distribution in multiply-stacked Si-QDs after charge injection, temporal change in surface potential after electron injection for the sample as seen in Fig. 5 (6-stacked Si-QDs in the gate oxide) was examined in an area without Al gate formation as shown in Fig. 6. A uniform surface potential was observed for the case without any bias applied to the surface. After scanning the sample surface with the AFM tip biased at +3V in the central part, a distinct decrease in the surface potential of the corresponding area, which is associated with electron injection to the dot, was observed. No change in the surface potential was detectable in the unbiased area. The result indicates thatt electrons are injected into the

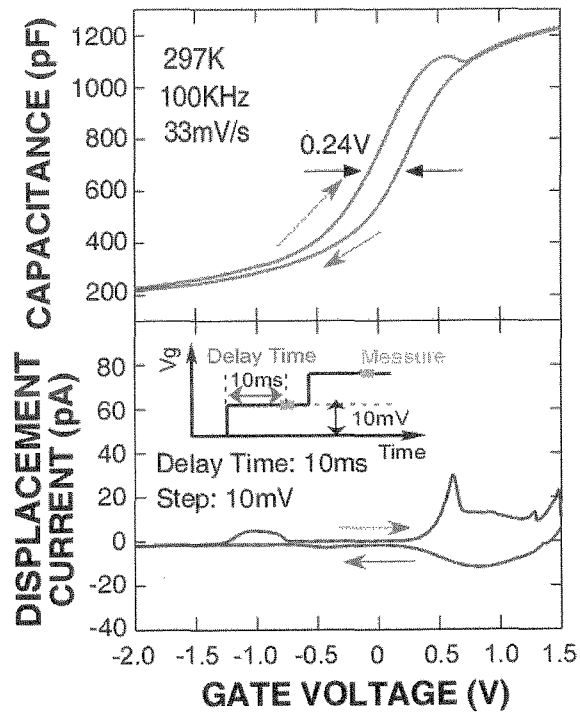

Fig. 5. Capacitance-voltage (a) and displacement current-voltage (b) characteristics of Al-gate MOS capacitors with 6 floating layers of Si dots on n-Si(100) measured at room temperature. The sweep rate for C-V measurements was 33 mV/s and for I-V measurements, the voltage step and the delay time were set at 10mV and 10 ms, respectively.

dots through the 4nm-thick bottom oxide from the n-Si(100) substrate. The surface potential change of 120mV just after electron injection was reduced to 65mV in 30 min after electron injection and to ~10mV in 60 min. However, no significant change of surface potential was observable between 60 min and 180 min after electron injection. In other words, the reduction in the surface potential tends to be saturated. Notice that the area charged with electrons spreads with time as seen in the progressively blurred surface potential image. This result indicates that injected electrons are displaced from the charged Si-QDs to the neighboring uncharged Si-QDs by Columbic repulsive force. Similar results were also obtained in the cases where electrons were extracted from the Si-QDs. Observed spatial spreading of injected charges is unique to multiply-stacked Si-QDs as high as ~10^{12} cm^{-2} between ultrathin SiO_2 interlayers, being hardly observed in a single Si-QDs array with a dot spacing larger than 4nm on SiO_2 [7].

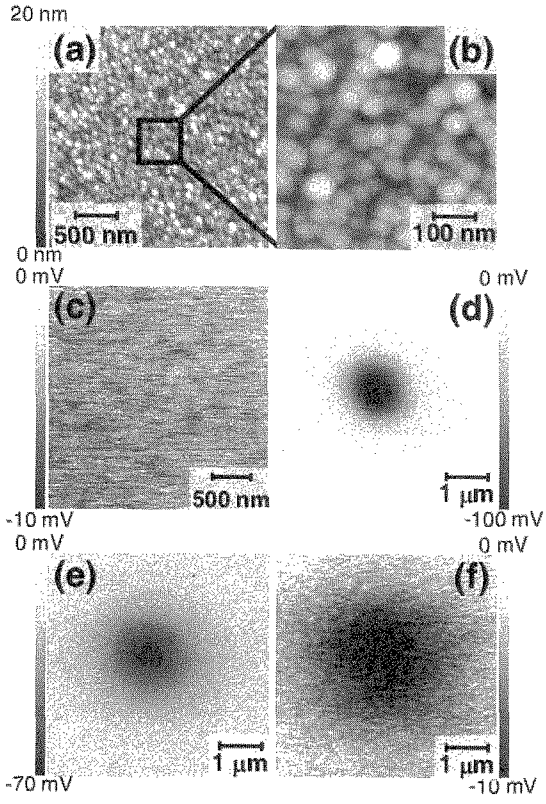

Fig. 6. Topographic image (a) and corresponding surface potential images of an area without Al gate formation of the sample shown in Fig. 5, measured by the Kelvin probe mode (b) before, (c) after electron injection with a tip bias applied at -3V (d) at the moment of injection, (e) 30 min and (f) 60 min after electron injection.

4. SUMMARY

We have demonstrated that a Si nucleation density as high as ~$6x10^{11}cm^{-2}$ can be achieved by remote Ar plasma and subsequent H_2 remote plasma just before SiH_4-LPCVD. The combination of LPCVD and remote plasma surface treatments including remote plasma oxidation is a promising method to fabricate multiply-stacked structures consisting of Si-QDs and ultrathin SiO_2 interlayers. From observing the charging and discharging characteristics of multiply-stacked Si-QDs in SiO_2, we suggested that plasma-induced damages and contaminations are negligible in this fabrication process. It is likely that the spacial spreading of injected charges in multiply-stacked Si-QDs is responsible for the temporal decay in the surface potential change after both electron injection and extraction.

ACKNOWLEDGEMENTS

This work was supported in part by Grant-in-Aids for scientific research of priority area (A) and the 21st Century COE program "Nanoelectronics for Terra-Bit Information Processing" from the Ministry of Education, Culture, Sports, Science and Technology of Japan.

REFERENCES

[1] S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E.F. Crabbe and K. Chan, Appl. Phys. Lett. 68 (1996) 1377.

[2] A. Kohno, H. Murakami, M. Ikeda, S. Miyazaki and M. Hirose, Jpn. J. Appl. Phys. 40 (2001) 721.

[3] M. Ikeda, Y. Shimizu, H. Murakami and S. Miyazaki, Jpn. J. Appl. Phys. 42 (2003) 4134.

[4] S. Miyazaki, Y. Hamamoto, E. Yoshida, M. Ikeda and M. Hirose, Thin Solid Films 369 (2000) 55.

[5] S. Miyazaki, M. Ikeda, E. Yoshida, N. Shimizu and M. Hirose, Proc. of 25th Int. Conf. on Phys. of Semicond., (Osaka, 2000) p. 373.

[6] J. Nishitani, K. Makihara, M. Ikeda, H. Murakami, S. Higasi and S. Miyazaki, Thin Solid Films (2005) in press.

[7] K. Makihara, H. Deki, H. Murakami, S. Higashi and S. Miyazaki, Appl. Surf. Sci. 244 (2005) p. 75.

[8] R.R. Irani and C.F. Callis in Particle Size Measurement: Interpretation and Application, (Wiley, New York, 1963).

[9] T. Shibaguchi, M. Ikeda, H. Murakami and S. Miyazaki, Tech. Dig. 2004 Asia-Pacific Workshop on Fundamentals and Application of Advanced Semiconductor Devices, (Nagasaki, 2004) p. 273.

(Received December 21, 2005; Accepted January 31, 2006)