Transactions of the Materials Research Society of Japan 31[1] 137-140 (2006)

Multistep Electron Charging to and Discharging from Silicon-Quantum-Dots Floating Gate in nMOSFETs

T. Nagai, M. Ikeda, Y. Shimizu, S. Higashi and S. Miyazaki
Graduate School of Advanced Sciences of Matter, Hiroshima University
Kagamiyama 1-3-1, Higashi-Hiroshima 739-8530, Japan
Phone: +81-824-24-7648, FAX: +81-824-22-7038, E-mail: semicon@hiroshima-u.ac.jp

The electronic charged states of Si-quantum-dots (Si-QDs) floating gate and their temporal changes have been studied systematically by measuring the transient variation of the drain current I_D (I_D-t) in n-metal-oxide-semiconductor field-effect-transistors after applying pulsed gate biases Vg. The threshold voltage increases stepwise with Vg pulse height, which indicates multistep electron charging in the Si-QDs floating gate due to the Coulomb blockade effect. I_D-t characteristics measured at zero gate bias, after applying pulsed gate biases for the dot floating gate to be charged, show that a critical transition from an unstable charged state to a stable charged state occurs dependent on the pulse height or width. This result suggests the redistribution of electrons in the floating gate during the metastable state, which involves a reduction in the effective charging energy and resultant elimination of the Coulomb blockade. We also observed similar multistep characteristics in electron discharging from Si-QDs floating gate. A change in the distribution of electrons also plays an important role in multistep electron discharging.

Key words: silicon quantum dot, multistep charging, multistep discharging, floating gate, Coulomb blockade

1. INTRODUCTION

The use of Si-QDs as a floating gate in metal-oxide-semiconductor field-effect-transistors (MOSFETs) has been attracting much attention because of its feasibility for multi-valued memory operations at room temperature [1-4]. One major concern in the implementation of a clear multi-valued function is the need for precise control of the discrete charged states in the Si-QDs gate, which are determined from the sum of charging energy and quantization energy of Si-QDs. Until now, we have fabricated nMOSFETs with a Si-QDs floating gate and confirmed multistep threshold voltage shift due to the Coulomb blockade effect of Si-QDs at room temperature [1, 4]. Also, we have demonstrated that electron charging of the Si-QDs floating gate at constant gate voltages proceeds stepwise through metastable charged states associated with the redistribution of injected electrons [4], and that the activation energies on the time for electron injection and the period in a metastable state were close to the sum of quantization energy and charging energy for the Si-QDs. This implies electron transfer between different energy states of neighboring Si-QDs [5]. Such unique multistep charging has yet to be studied in detail to control precisely the discrete charged states in the Si-QDs.

In this work, to gain a better understanding of the mechanism of the change of charged states in the Si-QDs floating gate, we examined the transient characteristics of the drain current after charging the Si-QDs floating gate at different pulsed gate biases, and the electron discharging characteristics of the Si-QDs floating gate.

2. EXPERIMENTAL

n-MOSFETs with a floating gate of doubly-stacked Si-QDs were fabricated by the following steps. Hemispherical and single-crystalline Si-QDs were self-assembled on a 3.3-nm-thick SiO_2 layer thermally grown on p-Si(100) by controlling the early stages of LPCVD of pure SiH_4 at 575°C. Next, a 1nm-thick thermal oxide layer was grown at 850°C, and the second Si-QDs layer was deposited under the same conditions. The average dot height and the dot density evaluated by AFM were 6nm and $6\times10^{11}cm^{-2}$, respectively. Subsequently, a 3.3nm-thick amorphous Si layer was uniformly grown on the dot layer by LPCVD of 10% Si_2H_6 diluted with He at 440°C and fully oxidized in dry 2% O_2 to form a 7.5-nm-thick control oxide. Finally, an n^+poly-Si gate and source/drain junction were fabricated. The gate length and width were typically 0.5 and 10μm, respectively.

3. RESULTS AND DISCUSSION

Figure 1 shows temporal changes in the drain current measured before and after application of single-pulsed gate biases at a base gate voltage of 0V. The drain current drops to the minimum value immediately after the application of pulsed gate bias. The minimum drain current corresponds to the amount of electrons injected by the pulse gate bias. As shown in Fig. 2, the minimum drain current decreases stepwise with increasing pulse height at different base gate voltages. Correspondingly, the threshold voltage shifts increase in a staircase pattern, indicating a multistep charging in the Si-QDs floating gate due to the Coulomb blockade effect.

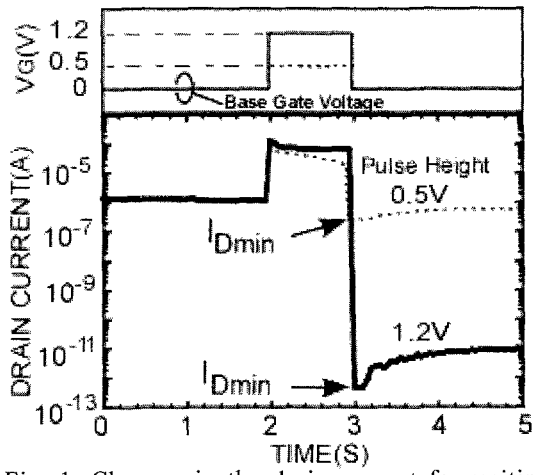

Fig. 1. Changes in the drain current for writing operations by applying a single-pulsed gate bias of 0.5 or 1.2V. The base gate voltage was set at 0V.

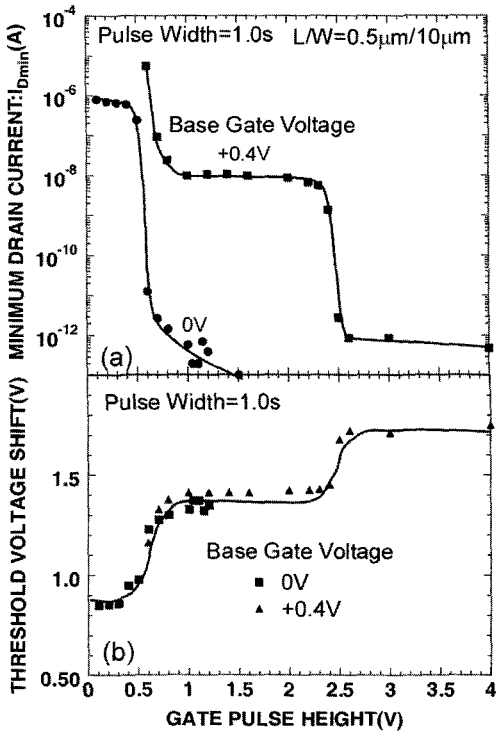

Fig. 2. (a) Minimum drain current and (b) threshold voltage shift as a function of gate pulse height at base gate voltages of 0 and +0.4V. The pulse width was constant at 1.0s.

Note that the threshold-voltage shift at each of the charging steps decreases with progressive electron charging. This implies that the Coulomb interaction among the neighboring charged Si-QDs contributes to an increase in the charging energy of the QDs.

To get a clearer insight into the charged states, the temporal change in the drain current was measured at a constant gate voltage of 0V after electron injection to the 2nd metastable state by

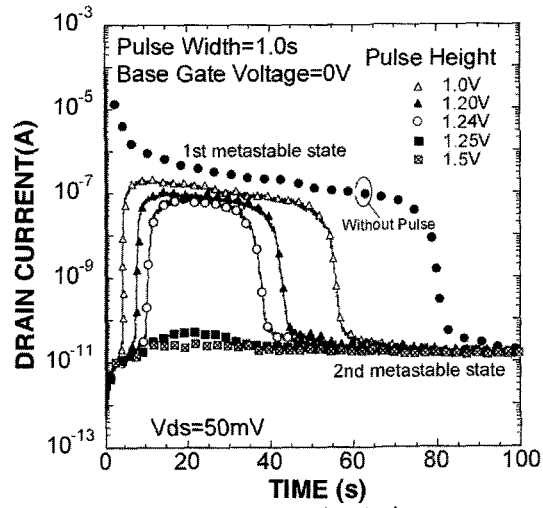

Fig. 3. Temporal changes in drain current at a gate voltage of 0V and a drain voltage of 50mV after applying different pulse gate biases. The pulse height was varied in the range of 1.0-1.5V at a constant pulse width of 1s. The result without application of any pulsed bias is also shown as a reference.

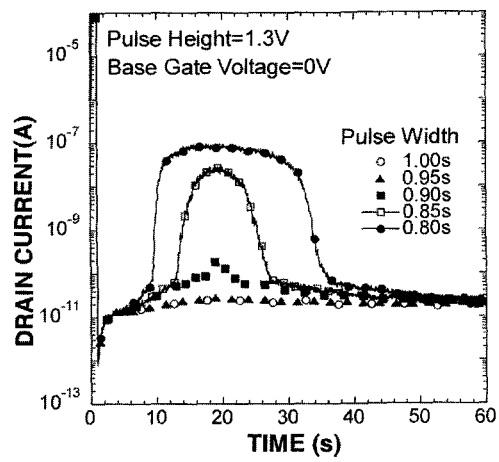

Fig. 4. Temporal changes in drain current at a gate voltage of 0V and a drain voltage of 50mV after applying different pulse gate biases. The pulse width was varied in the range of 0.8-1.0s at a pulse height of 1.3V.

applying the gate pulse bias as shown in Fig. 3. In cases with a pulse height of 1.24V and below, the drain current rapidly increases to a certain current level and then decreases as seen in the electron injection, without pulse except shortened time to the 2nd injected state. The increase in drain current indicates the emission of electrons stored in an unstable charged state of the Si-QDs floating gate. The emitted electrons were again injected in the Si-QDs floating gate via the metastable state. The metastable state, in which the drain current slightly decreases with time, is attributed to the redistribution of electrons remaining in the Si-QDs floating gate [4]. The length of the metastable state decreases with the pulse height. When the pulse height is

increased only by 10mV from 1.24V to 1.25V, an increase in the drain current due to electron emission with time is hardly observable, which indicates that injected electrons settle in a stable condition at V_G=0V. A similar result was obtained in the I_D-t characteristics after applying pulsed gate bias at different pulse widths and constant pulse height as shown in Fig. 4, where the electron emission after injection at a pulse height of 1.3V is observable within 0.90s in pulse width. The results of Figs. 3 and 4 indicate that pulse height and width are crucial factors for the charge distribution in the metastable state even though the amount of injected charge is the same at each pulse height.

We also investigated the discharging characteristics of the Si-QDs floating gate. Figure 5 shows the drain current versus gate voltage (I_D-V_G) characteristics of a Si-QDs floating gate MOSFET, which was measured as follows: After fully charging to the Si-QDs floating gate at V_G=+3V, the gate voltage was swept from +3V to a preset negative voltage and then swept back to +3V. The maximum negative gate voltages (V_{neg}) was varied in the range from -0.2 to -4.5V. With progressive

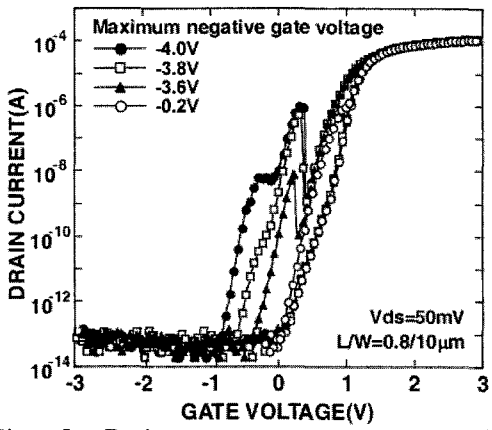

Fig. 5. Drain current versus gate voltage characteristics when the gate voltage was swept from +3V to the maximum negative voltage, which was preset at -0.2, -0.36, -0.38 or -0.4V, and then back to +3V.

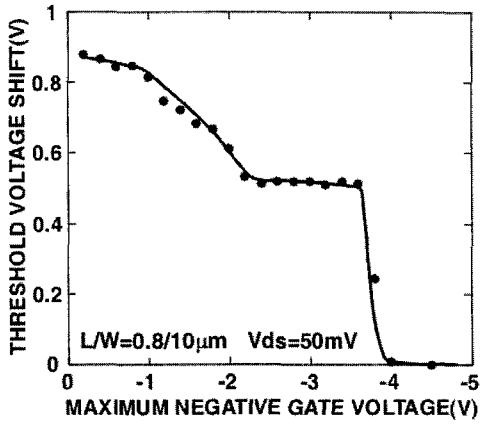

Fig. 6. Change in the threshold voltage shift as a function of the maximum negative gate voltage as seen in Fig. 5.

electron discharging from the Si-QDs floating gate at negative gate voltages, characteristic current bumps due to a multistep shift in threshold voltage become clearly observed in a backward sweep of the gate voltage toward the positive voltage side. As shown in Fig. 6, the threshold voltage shift caused by the application of negative gate voltages decreases stepwise with V_{neg} due to discharging of the Si-QDs floating gate. This result indicates the multistep electron discharging from the Si-QDs floating gate.

To gain insight into the discharge process, we also measured I_D-t characteristics after partial discharging as shown in Fig. 7. In this measurement, the Si-QDs floating gate was discharged for a length of time (50s in Fig. 7) at a certain negative V_G (–1V in Fig. 7) after being fully charged at +3V, and then gate voltage was switched from –1V to 0V to evaluate the threshold voltage. Just after gate voltage was switched to 0V, drain current was increased immediately to maximum drain current and then decreased due to the electron charging of the Si-QDs floating gate. The maximum drain current reflects progress in the discharging of the Si-QDs floating gate. We summarized the maximum drain current as a function of discharging time at discharging voltages in the range from -0.2 to -1.4V as

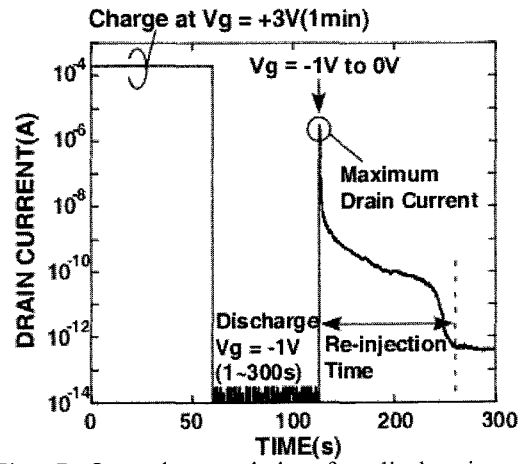

Fig. 7. I_D-t characteristics for discharging at V_G=–1V after being fully charged at +3V and re-injection at V_G=0V.

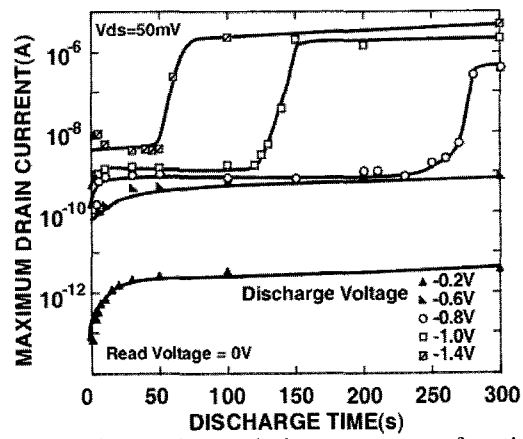

Fig. 8. The maximum drain current as a function of discharge time. The discharging voltage was varied from -0.2 to -1.4V.

shown in Fig. 8. For discharging voltages ranging from -0.2 to -0.6V, the maximum drain current gradually increases with discharging time and is saturated at the current level between the 1st and 2nd charged state at V_G=0V. For discharging voltages of -0.8V and over, the maximum drain current increases stepwise, reflecting discharging in the Si-QDs floating gate fully through an intermediate state close to the 1st charged state. In the intermediate state, since the maximum drain current is almost constant with respect to discharging time, the amount of charge in the Si-QDs floating gate remains unchanged. This result suggests a change in electron distribution in the Si-QDs floating gate during the intermediate state, as in the case of electron charging. Figure 9 shows the maximum drain current plotted as a function of re-injection time. Even in the cases with almost the same amount of electrons in the Si-QDs floating gate, the time for re-injection from the first charged state to 2nd charged state was markedly different, presumably depending on the electron distribution in the floating gate. When the Si-QDs floating gate is discharged beyond the first charged state, re-injection time is almost constant independent of the maximum drain current. This is because the injection time to the 1st charged state is quite short compared with the period of the metastable state to the 2nd charged states.

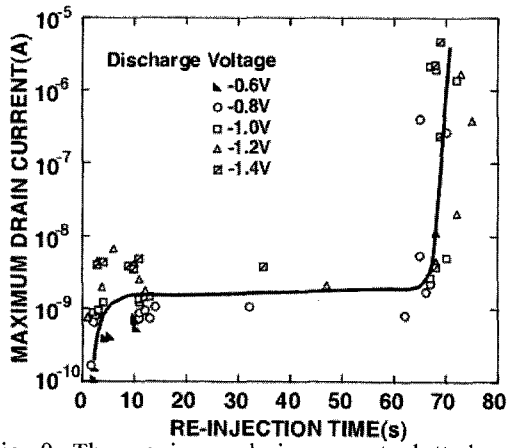

Fig. 9. The maximum drain current plotted as a function of re-injection time at V_G = 0V after partially discharged in the gate voltage range from -0.6 to -1.4V.

4. SUMMARY

The temporal change in the drain current after applying pulsed gate biases confirms the redistribution of electrons in the Si-QDs floating gate during the metastable state, which involves a reduction in the effective charging energy and a release of the Coulomb blockade. Similarly, discharging from the pre-charged Si-QDs floating gate proceeds stepwise, which is also interpreted in terms of the electron redistribution.

ACKNOWLEDGEMENTS

This work has been supported in part by a Grant-in-Aid for the 21st Century COE program "Nano Electronics for Tera-bit Information Processing" from the Ministry of Education, Science, Sports and Culture of Japan.

References

[1] A. Kohno, H. Murakami, M. Ikeda, S. Miyazaki and M. Hirose: Jpn. J. Appl. Phys. 40 (2001) L721.

[2] I. Kim, S. Han, K. Han, J. Lee and H. Shin: Jpn. J. Appl. Phys. 40 (2001) 447.

[3] E. Kapetanakis, P. Normand, D. Tsoukakas and K. Beltsios: Appl. Phys. Lett. 80 (2002) 2794.

[4] M. Ikeda, Y. Shimizu, H. Murakami and S. Miyazaki: Jpn. J. Appl. Phys. 42 (2003) 4134.

[5] M. Ikeda, Y. Shimizu, T. Shibaguchi, H. Murakami and S. Miyazaki: Ext. Abst. of the 2003 Intern. Conf. on Solid State Devices and Materials (Tokyo, 2003) p. 846.

(Received December 26, 2005; Accepted January 31, 2006)