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Statistical Evaluation of Very Low Gate Leakage Current for Bit Error Evaluation in Flash Memory

Tomoyuki Suwa[1], Shigetoshi Sugawa[1], Hiroto Takahashi[1], Akinobu Teramoto[2] and Tadahiro Ohmi[2]
[1]Graduate School of Engineering, Tohoku University
[2]New Industry Creation Hatchery Center (NICHe), Tohoku University
Aza-Aoba 10, Aramaki, Aobaku, Sendai, 980-8579, Japan
Fax: 81-22-795-3977, e-mail: suwa@fff.niche.tohoku.ac.jp

Leakage current through tunnel oxides is characterized as very localized and of very low current. The leakage current has been conventionally measured in relatively large area capacitors or transistors; as a result, localized and low leakage current cannot be measured. Therefore, it is required that very localized and very low leakage current is measured for many samples in a short time for bit error evaluation. In this paper, we propose the new concept TEG for bit error evaluation. The very small leakage current is integrated by capacity in each cell, and it is detected in high sensitivity as a voltage signal. This TEG is manufactured by a very simple process (1Poly, 1Metal) and very small gate area (< 1um^2). It is possible to measure very low gate leakage current (>10^{-17}A), and the large number of cells can be measured in a very short time (8Kbit measurement finish within tens of seconds). In addition, F-N electron injection stress, which is the equivalent of the operations (read, write, erase) of flash memory, can be applied to all cells at the same time. We statistically evaluated the Stress Induced Leakage Current (SILC).
Key words: SILC, Flash-memory, Bit-error, tunnel-oxide

1. INTRODUCTION

As flash memory cell size is scaled down, the down-scaling of tunnel oxide thickness is one of the most effective components for reducing applied voltage and cell size. However, it has been reported that the down-scaling of tunnel oxide thickness is limited by degradation of oxide quality, which is characterized by the stress-induced leakage current (SILC)[1] that occurs after the write/erase cycling of the flash memory cell. Furthermore, few cells exhibit an anomalous SILC, leading to bit error in flash memory [2-7]. Therefore the reliability of flash memory with down-scaling of the tunnel oxide is limited by the anomalous leakage current of very few cells [8]. The leakage current of such cells is characterized as very localized and very low current. In this paper, we propose a new concept, test element group (TEG), for the bit error evaluation, and measured a large number of cells and a very localized leakage current in a very short time.

2. NEW CONCEPT TEG

Figure 1 shows the schematic of the circuit of a unit cell in the array TEG that we proposed. The transistor in the solid line circle is the tunnel gate transistor for measuring the gate leakage current, and the gate area of this transistor is 1um^2. Stress-inducing circuits are connected with the source and drain of the tunnel gate transistor. These circuits can be applied to F-N electron or hot electron injection stresses, which are equivalent to flash memory operations (read, write and erase).

When we designed this circuit, we incorporated two important circuit techniques. First, the gate leakage current is integrated by the capacitor (C=10fF) in the doted line circle. It is hard to measure the gate leakage current directly because it is a very low current due to the very small tunnel gate area. Therefore, the gate leakage current is converted to the voltage signal by the capacitor in each cell. The converted voltage signal is read by using the source follower circuit. Secondly, the common-gate circuit is connected between the tunnel gate transistor and the capacitor. If the electric field in the tunnel oxide changes during the integration period, the gate leakage current cannot be evaluated accurately. When the gate bias (Vg) is positive, the PMOS-FET of the common-gate circuit is turned on. On the other hand, when the gate bias (Vg) is negative, the NMOS-FET is turned on. For example, when Vg is positive, the bias point V_{sd} is almost determined by $V_{RP}+V_{th}$. Therefore, the electric field in the tunnel oxide is independent of the integrated charge in the capacitor.

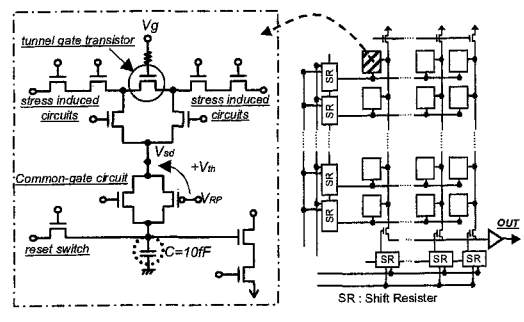


Fig. 1. A circuit schematic of a unit cell and cell array.

Figure 2 shows a schematic view of the gate leakage current flows. It is possible to measure the current which flows between gate and channel and between gate and source/drain by switching the MOSFETs connected source or drain. In addition, the direction of the gate leakage current can be changed by changing the polarity

of Vg. This unit cell is arrayed by 8192 cells. The voltage signal is sequentially read by using shift register circuits.

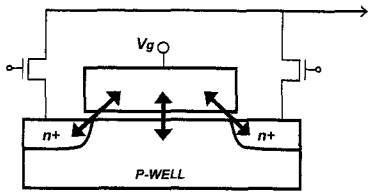


Fig. 2. A schematic view of the gate leakage current flows.

Figure 3(a)-(c) show the circuit operations of a unit cell. First, in Fig. 3(a), the gate leakage current flows and the voltage of the capacitor is set at a constant voltage (V_{RES}). Secondly, in Fig. 3(b), the reset switch is turned off and the leakage current is accumulated in the capacitor during the accumulation time (t). Finally, in Fig. 3(c), the voltage signals are sequentially read.

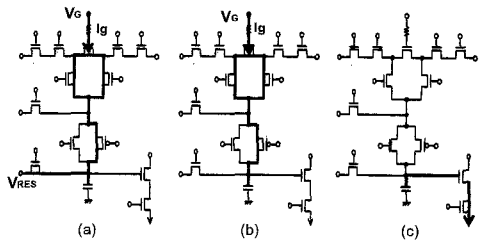


Fig. 3. The circuit operations of a unit cell.
(a) The voltage of the capacitor is reset by the reset voltage (V_{RES}).
(b) The integrated capacitor is accumulated by the gate leakage current.
(c) The voltage signals are sequentially read.

The measurement sequence is as follows. First, the background leakage current is integrated by the capacitor on all cells at the same time. The background leakage current is characterized as a leakage current other than the gate leakage current, for example, a pn junction leakage current. The voltage signal (V_0) converted by the background leakage current is then sequentially read. Second, the background and the gate leakage current are integrated by the capacitor on all cells at the same time. The voltage signal (V_1) converted by the background and gate leakage currents is then sequentially read. Finally, the difference between V_1 and V_0 is calculated, and the gate leakage current is calculated by the following equation.

$$I_g = \frac{V_1 - V_0}{t} \times C$$

3. EXPERIMENTS

Experiments were carried out on a TEG fabricated using 0.35um 1Poly 1Metal CMOS technology. The tunnel oxide thickness was 7.0 nm and the tunnel oxide area was about 0.73um^2. Figure 4 shows the schematic of the tunnel gate transistor of the F-N stress condition. Electrons were injected from the substrate and the constant stress voltage was 8.0V. A measurement was finished in a few seconds.

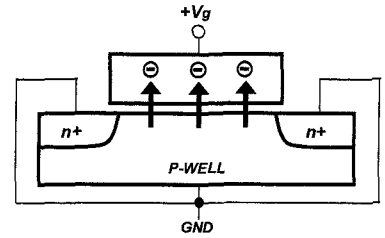


Fig. 4. A schematic view of the tunnel gate transistor of the stress condition.

4. RESULTS AND DISCUSSION

Figures 5-7 show the distribution of the gate leakage current at 5.6V, 5.7V and 5.9V, respectively. These figures show the distribution of the gate leakage current (a) before stress and (b) after a stress accumulation time of 1000 sec. After stress, the number of tail cells which have larger current than main distribution is increased, and the gate leakage current of the main distribution shows a shift to a lower current direction. This is considered that the existence of tail cells means a detection of an anomalous SILC and the main distribution shift is caused by the electron traps that exist in the tunnel oxide film.

Figure 8 shows a comparison of the average SILC and the anomalous SILC, and shows J-E characteristics in a large area (10^{-4}cm^2) capacitor. The average SILC is the current value of the summation of all cells. The magnitude of the average SILC is similar to that SILC measured by in the large area capacitor. The current density of the anomalous SILC is much larger than that of the average SILC. However the anomalous SILC is very local. Therefore, the magnitude of the anomalous SILC is very small. It is suggested that the anomalous SILC is buried in average SILC in the conventional measurement in the large area capacitor, and it becomes necessary to measure by the large number of cells with very small tunnel oxide area for bit error evaluation attributed the anomalous SILC.

Figures 9-11 show the dependence of the SILC at 5.6V, 5.7V and 5.9V, respectively on the stress accumulation time. The gate leakage current characteristics are largely changed by cells after the F-N electron injection stress. It is considered that the gate leakage current characteristics easily change by the influence of the electron and hole trap or detrap in the tunnel oxide film due to the measurement of the very localized leakage current through the very small tunnel oxide area.

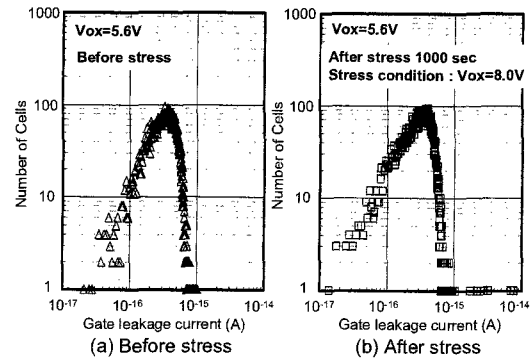
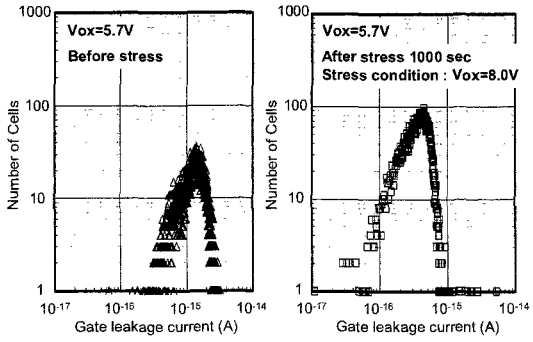
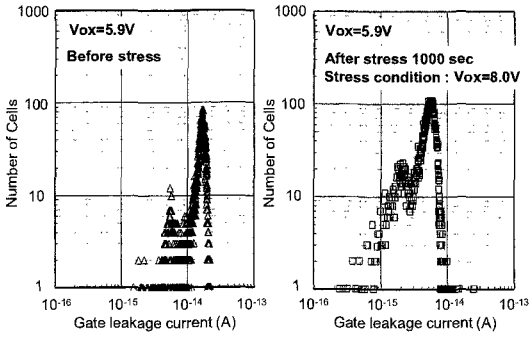


Fig. 5. Distribution of the gate leakage current at 5.6V.



(a) Before stress (b) After stress

Fig. 6. Distribution of the gate leakage current at 5.7V.



(a) Before stress (b) After stress

Fig. 7. Distribution of the gate leakage current at 5.9V.

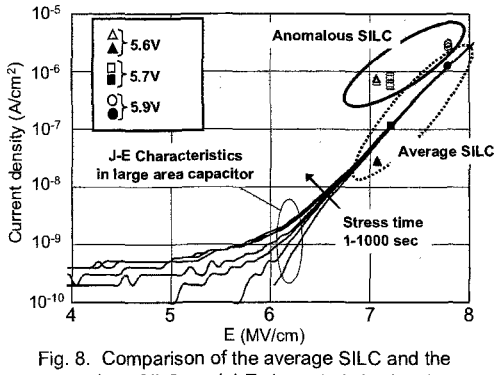


Fig. 8. Comparison of the average SILC and the anomalous SILC, and J-E characteristics in a large area capacitor.

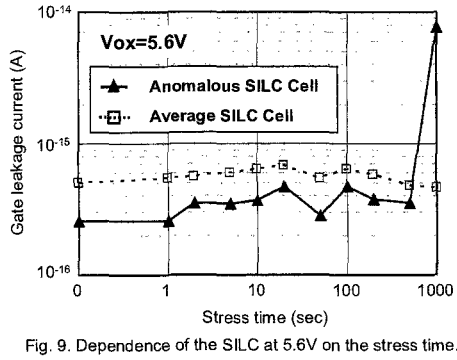


Fig. 9. Dependence of the SILC at 5.6V on the stress time.

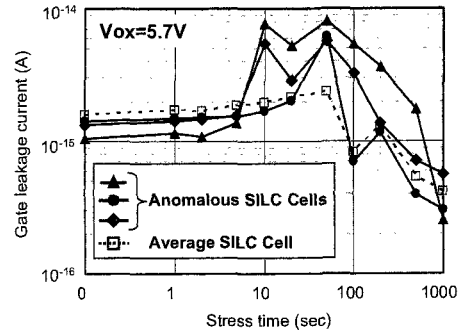


Fig. 10. Dependence of the SILC at 5.7V on the stress time.

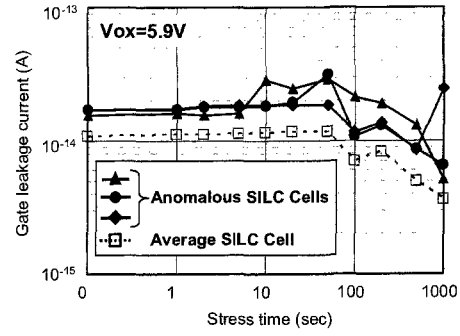


Fig. 11. Dependence of the SILC at 5.9V on the stress time.

5. CONCLUSION

We proposed a new concept TEG for bit error evaluation and measured a large number of cells and a very localized leakage current in a very short time. By using this TEG, we found a few cells which have localized and anomalous SILC. The value of anomalous SILC is ten times or more larger than the value of the average SILC. A very localized and anomalous SILC cannot be observed by direct measurement of the current in a large area capacitor, which only gives averaged information.

We have shown the measurement of gate leakage current characteristics by using a new concept TEG is a powerful tool in developing flash memory with down-scaled tunnel oxide thickness because it is possible to investigate the anomalous SILC at a microscopic level in a very short time and through a very simple process.

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