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Low Temperature Deposition of Silicon Nano-dots by PECVD

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We have developed plasma-enhanced chemical vapor deposition (PECVD) methods and investigated the optimum process conditions for forming SiO_2 films and Si dots below 430°C. A conductively coupled plasma (CCP) source with the side-wall electrode and an inductively coupled plasma (ICP) source with internal low-inductance antennas (LIAs) were used to deposit SiO_2 films and Si dots, respectively. Electronic properties were examined with capacitance-voltage (C-V) and current-voltage (I-V) measurements for the CVD-SiO_2 film and fabricated metal oxide semiconductor (MOS) capacitor. The result showed electronic characteristics of CVD-SiO_2 equal to those of thermal oxide and the memory operation due to electron charging to the dots.
Key words: nano-dot, SiO_2, PECVD, CCP, ICP

1. INTRODUCTION

The silicon nano-dot (Si dot) is a promising material for new functional devices because it exhibits unique features, such as coulomb blockade, light emission and absorption [1 - 3]. Many studies to produce Si dots have been performed at rather high temperature [4]. However, treatment at lower temperature is desirable for usage of substrates that consist of low melting point materials. In addition, high through-put and coverage would be required in terms of mass formation.

In this work, we aimed to deposit SiO_2 films and nano-dots by adapting the plasma-enhanced chemical vapor deposition (PECVD) method that we have developed for low temperature micro-crystalline silicon transistors. PECVD has been widely used for preparing thin films because of its high deposition rate and large coverage. On the other hand, there are well-known weak points such as the damage caused by the plasma impact and the difficulty of the control. In order to resolve these problems, we developed two kinds of plasma sources, a conductively coupled plasma (CCP) source with side-wall electrode [5] and an inductively coupled plasma (ICP) source with an internal low-inductance antenna (LIA) unit [6,7]. The former was used for the deposition of SiO_2 films because material gases, SiH_4 and O_2, could be uniformly introduced into the process chamber through the shower plate which faces the substrate. The latter was used for the formation of Si-dots utilizing high-density and low-potential hydrogen plasma.

The structural and electronic properties of SiO_2 film and Si-dots were individually evaluated by means of field emission scanning electron microscope (FE-SEM), transmission electron microscope (TEM), ultra-violet (UV) Raman spectrometry, photoluminescence (PL) spectroscopy, capacitance-voltage (C-V) and current-voltage (I-V) measurements. The electronic characteristics of fabricated devices (Si dot MOS capacitors) were also examined.

2. EXPERIMENTAL

2.1 SiO_2 deposition

A schematic diagram of the experimental setup for the deposition of SiO_2 films is shown in Fig. 1. The side-wall type electrode was divided into four pieces and very high frequency (VHF, 60 MHz) power was supplied through the matching circuit units (matching box) at each corner of the process chamber. Attainable vacuum degree was less than 10^{-4} Pa. The area of the substrate was 600 mm × 720 mm.

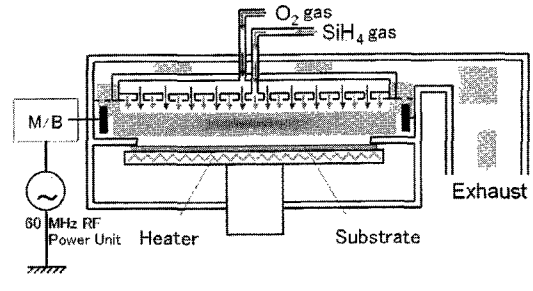

Fig. 1. The experimental setup of the CCP-CVD apparatus for the deposition of SiO_2 films. Here M/B means Matching Box.

2.2 Si dot formation

Si dot formation was carried out with the apparatus shown in Fig. 2. Eight antenna conductors were set in a vacuum container to eliminate the need for insulating partitions so that

the induced electric field from an antenna could be used effectively. By reducing the antenna inductance and fully covering the antenna conductors with insulator, the plasma potential would decrease and thus the plasma damage could be suppressed. The excitation frequency was 13.56MHz. Attainable vacuum degree was equal to that of the apparatus for SiO_2.

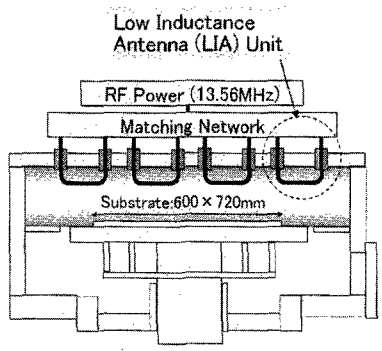

Fig. 2. The experimental setup of the ICP-CVD apparatus for the formation of Si dots.

3. RESULTS AND DISCUSSION

3.1 SiO_2 properties

As mentioned above, the electronic properties of SiO_2 films deeply affect the characteristics of Si dot devices as well as those of the Si dot itself. At first, therefore, we searched for the optimum condition for producing SiO_2 films. The predominant conditions are summarized in Table I.

Table I. Conditions of SiO_2 deposition.

Flow rate (ccm)	SiH_4	300
	O_2	500 - 2000
RF power (W)		4000 (1000×4)
Deposition temperature (°C)		400
Total gas pressure (Pa)		6.7

Figures 3 and 4 show the C-V and I-V characteristics of SiO_2 films. It was found that CVD-SiO_2 films equal the thermal oxide in the interface state density and the dielectric break-down voltage under the condition that the ratio of the net flow rates SiH_4/O_2 = 300/2000 ccm. From this result, we confirmed that the quality of SiO_2 films deposited by the side-wall type CCP-CVD could be used as control oxides of Si dot devices.

It is worth noting that we planned for the SiO_2 deposition by the same method as that of the Si dot formation mentioned in the next section in order to take full advantage of the lower plasma potential and higher plasma density.

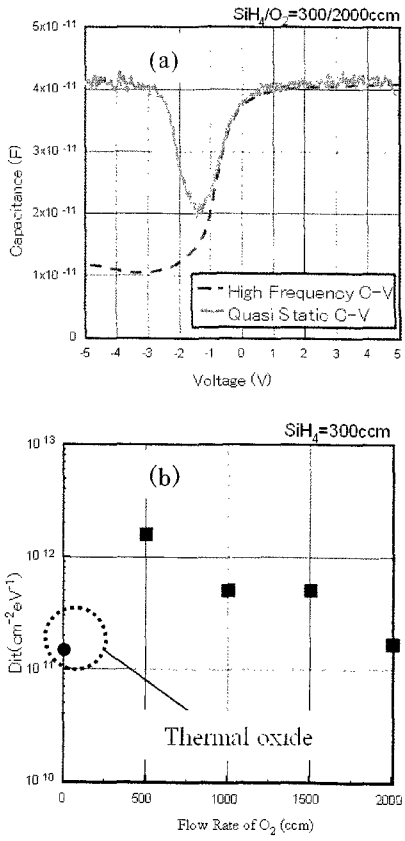

Fig. 3. (a) C-V characteristics of a CVD-SiO_2 film (this work) and (b) induced interface state density of CVD-SiO_2 and thermal oxide.

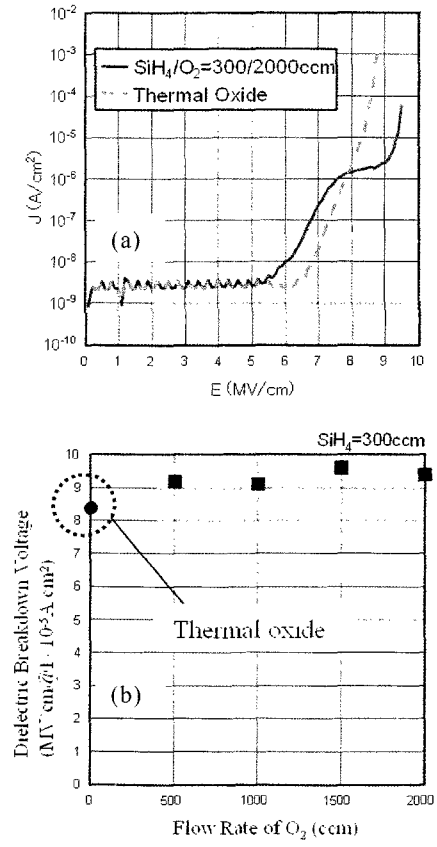

Fig. 4. (a) I-V characteristics of CVD-SiO_2 and thermal oxide films and (b) induced dielectric break-down voltage.

3.2 Si dot properties

The Si dots were formed on the thermal oxidation layer (3 nm) of n-type (100) Si substrate for FE-SEM. The samples with successive two-step depositions. Si dots and then CVD-SiO_2, on the same substrate as mentioned above were made for TEM observation, and C-V and I-V measurements of the MOS capacitor. In addition, samples simultaneously deposited on fused quartz substrates were prepared for PL observation. The area of the substrates was approximately 20 mm × 20 mm. Si dots were formed at different deposition temperatures ranging from 250 to 430°C, using a SiH_4/H_2 gas mixture. Other formation conditions were fixed and are summarized in Table II.

Table II. Conditions of Si dot formation.

Flow rate (ccm)	SiH_4	1
	H_2	150
RF power (W)		10000 (2500×8)
Deposition temperature (°C)		250 - 430
Total gas pressure (Pa)		6.7

SEM images of the dot deposited at various temperatures are shown in Fig. 5. Sizes and densities estimated from these figures are summarized in Table III. It was found that the dot density and uniformity improved with decreasing temperatures. To explain this dependence, we considered that the increase of the temperature of the substrate leads to the progress of the migration of Si atoms and their aggregation. Therefore, the average diameter and dispersion of Si dots should be larger. The resultant dots were observed by TEM images as shown in Fig. 6.

Figure 7 shows the UV Raman spectra of Si dots grown at various temperatures. Crystallinity depended on the deposition temperature and the Raman peak of the sample grown at 300°C showed the best crystallinity close to the bulk Si. Further investigations, such as the correlation between the signature in the UV Raman spectrum and the PL intensity are now in progress. Some literature suggests that the strongest PL is observed for the samples with less-defined crystallization like the spectrum at 250°C in Fig. 7 [8,9].

Table III. Sizes and densities of Si dots.

Deposition temperature (°C)	Dot density (dots/cm^2)	Dot size (nm)
430	8.5×10^{11}	7.2 (σ = 0.8)
300	8.8×10^{11}	7.7 (σ = 0.7)
250	9.3×10^{11}	6.9 (σ = 0.5)

Figure 8 (a) and (b) show the C-V characteristics of the MOS capacitors without and with dots, respectively [10]. In the capacitor without dots, hysteresis was not confirmed. On the other hand, various hysteresis curves were observed depending on the deposition temperature. These observations of hysteresis curves suggest the electron injection into the dots. We could confirm the amounts of the voltage shift depended on the deposition temperature. Except for the dot deposited at 250°C, n_e (the number of electrons in a dot) estimated from ΔVth is one electron/dot; however, n_e of the dot deposited at 250°C is estimated to be more. It is suggested that the electrons are confined in other parts of the dot, e.g., in interface levels between the dot and the control oxide.

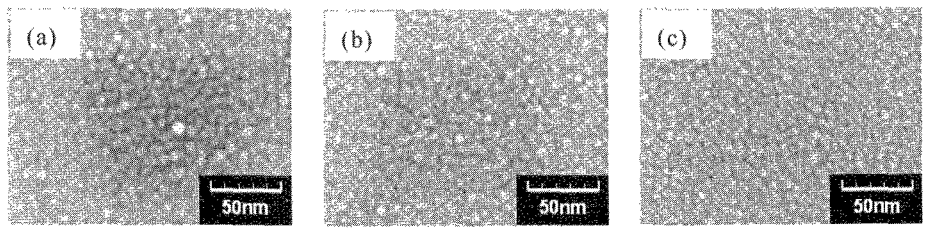

Fig. 5. SEM images of Si dots formed on Si substrates with 3 nm thermal oxide at (a) 430°C, (b) 300°C and (c) 250°C.

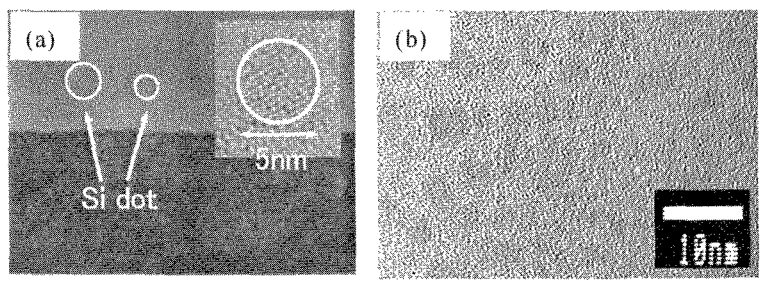

Fig. 6. (a) Cross-sectional and (b) plane-view TEM images of Si dots grown on the thermal oxidation layer of single crystal Si substrate and embedded in a SiO_2 matrix.

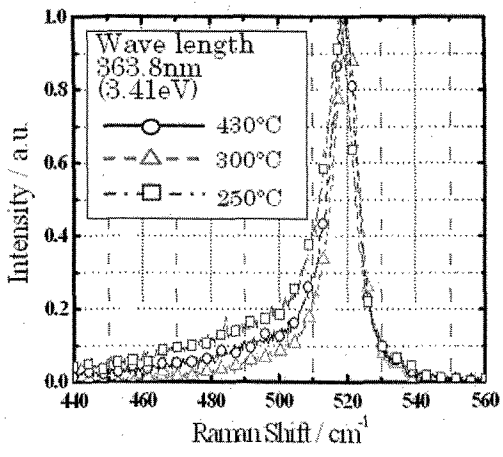

Fig. 7. UV Raman spectra of Si dot samples grown at 430°C, 300°C and 250°C.

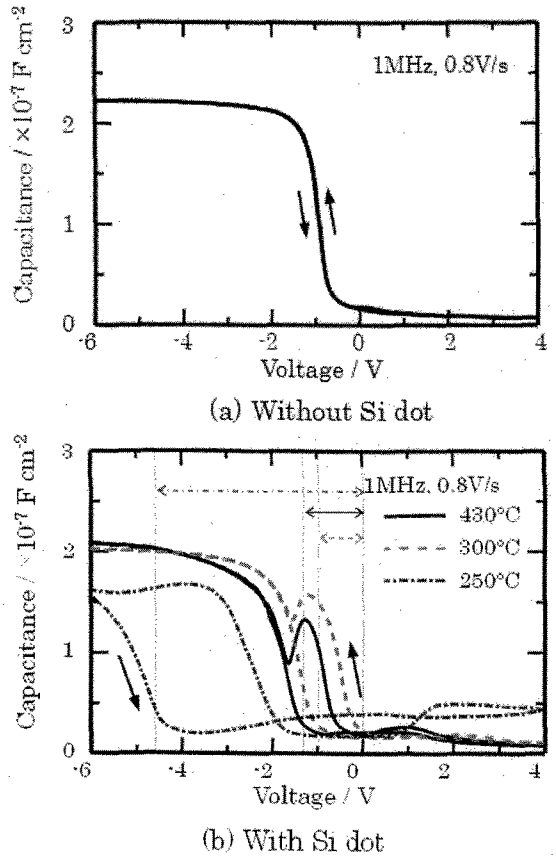

Fig. 8. High frequency C-V characteristics of MOS capacitors (a) without Si dot, and (b) with Si dot.

4. CONCLUSION

We investigated SiO_2 deposition and Si nano-dot formation by improved PECVD methods at low temperature. The density and the distribution of the diameter of Si dots could be changed by the formation temperature. It was also found that morphology and crystallinity of the dot depends on the temperature. Even for temperatures below 430°C, SiO_2 films show that the good performance and memory effect of the Si dot MOS capacitor could be confirmed. This result suggests that the Si dot can be applied to the memory devices.

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