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Fabrication of SBT-based Ferroelectric Thin Films for Low Voltage Operation of Ferroelectric-gate FET

Hirokazu Saiki, Syahhibul Azwar and Eisuke Tokumitsu
Precision and Intelligence Laboratory, 4259-R2-19 Nagatsuta, Midori-ku, Yokohama, Kanagawa, 226-8503 Japan
Fax: 81-45-924-5084, e-mail: saiki@neuro.pi.titech.ac.jp

Ferroelectric $(Sr,Sm)_{0.8}Bi_{2.2}Ta_2O_9$ (SSBT) thin films were fabricated for low voltage operation of ferroelectric-gate field-effect transistors (FET). It is demonstrated that SSBT films have smaller remanent polarization than conventional $Sr_{0.8}Bi_{2.2}Ta_2O_9$ (SBT) films, which is suitable to ferroelectric-gate FET applications. We also demonstrate low voltage operation (<5V) of ferroelectric-gate FET using ferroelectric SSBT film. We fabricated n-channel ferroelectric-gate FETs with $Pt/Sr_{0.7}Sm_{0.07}Bi_{2.2}Ta_2O_9$(170nm) /$HfO_2$(15nm)/Si structures. The drain current – gate voltage characteristics exhibit clear hysteresis loops due to the ferroelectric-gate insulator. A memory window of 0.54V was obtained with a gate voltage (V_G) sweep of ±5V and the constant drain voltage (V_D) of 0.1V. The ON/OFF current ratio was more than 10^3 in V_G=0.4V. We also demonstrate that the ON/OF current ratio is reduced to 10^2 at the read-our operation.

Key words: ferroelectric random access memory (FeRAM), ferroelectric-gate transistor, low voltage operation, read-our operation, $Sr_{0.8}Bi_{2.2}Ta_2O_9$ (SBT), $(Sr,Sm)_{0.8}Bi_{2.2}Ta_2O_9$ (SSBT)

1. INTRODUCTION

Recently, FeRAM[1-3] (ferroelectric random access memory) has attracted much interest because FeRAM has promising characteristics such as non-volatility, high-speed, and low power consumption. Generally speaking, there are two types in FeRAM. One is the 1T1C-type, whose memory cell is composed of 1 transistor and 1 capacitor, and the other is the 1T-type, whose memory cell is composed of only 1 transistor. Present FeRAMs are the 1T1C-type and are applied to niche markets such as ID cards, embedded memory applications, and so on. At present, the memory densities of FeRAMs in mass production and in laboratory developments (prototypes) are 1 MBits and 64 MBits, respectively. However, 1T1C-FeRAMs have a problem of further scaling, i.e., the scaling down the memory cell size decreases the ferroelectric capacitor size, which significantly reduces the absolute value of the switching charge, and hence the ON/OFF margin will decrease.

On the contrary, 1T-type FeRAMs[4-7] do not have such a problem because the ON/OFF states are detected by the drain current of ferroelectric-gate FET, whose gate insulator is a ferroelectric thin film. In this case, the charge per unit area is an important parameter; hence, scaling does not affect the ON/OFF margin directly. Therefore, research and development in 1T-type FeRAM is in high demand for future FeRAMs.

Although previous reports on ferroelectric-gate FETs revealed many problems such as the ferroelectric/ semiconductor interface[8] and short retention time, Aizawa[9] and Sakai[10] recently reported excellent electrical properties. Both groups adopted MFIS (metal-ferroelectric-insulator-semiconductor) structured FETs. However, these devices still need relatively high operation voltages because relatively thick ferroelectric layers are used in their devices.

In this paper, we first discuss the required electrical properties of ferroelectric thin films especially for low voltage operation. Next, we demonstrate that the newly developed $(Sr,Sm)_{0.8}Bi_{2.2}Ta_2O_9$ (SSBT) thin films have smaller remanent polarization than conventional $Sr_{0.8}Bi_{2.2}Ta_2O_9$ (SBT) films, which is suitable to ferroelectric-gate FET applications. MFIS-FETs with $Pt/Sr_{0.7}Sm_{0.07}Bi_{2.2}Ta_2O_9$(170nm)/$HfO_2$(15nm)/Si structures were then fabricated and characterized, and finally, low voltage operation was examined for the fabricated ferroelectrc-gate FETs with SSBT films.

2. THEORETICAL CONSIDERATIONS

It is important to note that the ferroelectric-gate transistor requires two characteristics for the ferroelectric film: a small remanent polarization (<2μC/cm^2) and well-saturated polarization-voltage (P-V) hysteresis loops. The polarization of the ferroelectric-gate insulator should match the channel charge of the FET, which is usually less than 2 μC/cm^2. However, the polarization of conventional ferroelectric materials, such as SBT and $Pb(Zr,Ti)O_3$ (PZT), is 10-30 μC/cm^2. Hence, it would be beneficial if a new ferroelectric material with small remanent polarization was developed for MFIS-type ferroelectric-gate transistors.

Furthermore, "saturation" of the P-V loops is also important especially for the low-voltage operation. Figure 1 shows examples of the P-V hysteresis loops of the ferroelectric thin films. It is found that minor loops (P-V loops when the applied voltage is small) for the ferroelectric film shown in Fig. 1(a) are wider than those for the film shown in Fig. 1(b). Here, we call such hysteresis loops shown in Fig. 1(a) and Fig. 1(b), well-saturated and poorly-saturated hysteresis loops, respectively. Figure 2 explains the operation of the MFIS-FET. When a certain voltage V_G is applied to the gate of MFIS-FET, the voltage of the ferroelectric capacitor V_F and that of the insulator V_I ($=V_G-V_F$) are determined so as to induce the same charge for the both capacitors. Hence, we can depict the Q-V_I relation of the

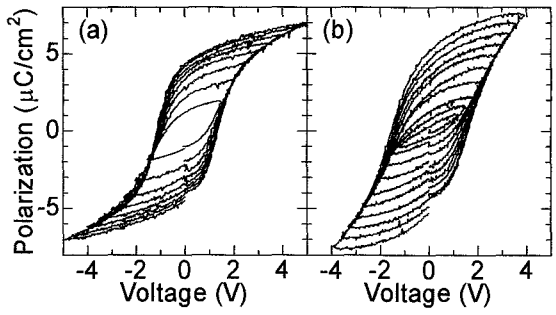

Fig. 1. P-V hysteresis loops of the ferroelectric films, (a) well- and (b) poorly-saturated P-V loops.

"I" layer on the Q(=P)-V_F hysteresis loops as a load line, because V_I=V_G-V_F. The intersection of the P-V hysteresis and the load line gives us an operating point of the device. When V_G increases, the load line moves to the right and the operation point moves along the hysteresis loop. If the operation point is in the upper left slope (inversion region) of the load line, the MFIS-FET is in ON state as shown in Fig. 2(a). On the other hand, if the operation point is in the lower right slope (accumulation region) or middle flat region (depletion region), the MFIS-FET is in OFF state as shown in Fig. 2(b). Note that the memory window of the MFIS-FET is given by the width of the hysteresis loops. Even when the ferroelectric film with a small remanent polarization is used, it is expected that the operation point is on one of the minor loops when the applied voltage is low. Therefore, to obtain a large memory window in the low voltage operation, it is important for the ferroelectric film has wide minor loops, namely well-saturated hysteresis loops.

In this paper, the feasibility of Sm-doped SBT (SSBT) film was examined for low voltage operation of the ferroelectric-gate FET, because we have previously found that SSBT has a small remanent polarization (~2μC/cm²)[12].

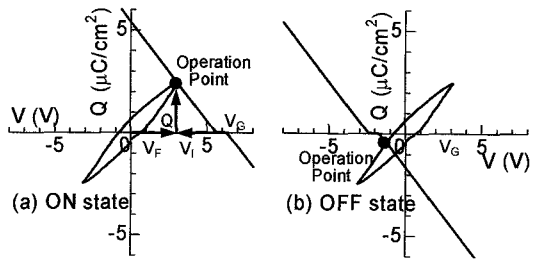

Fig. 2 Load-line analysis of n-ch MFIS-FET in (a) the ON state and (b) the OFF state.

3. EXPERIMENTAL PROCEDURE

Fabrication processes for the SBT/SSBT capacitors and ferroelectric-gate FETs are shown in Table I and Table II, respectively. Note that the SSBT films were fabricated by the sol-gel technique, in which we performed layer-by-layer crystallization at 750°C in oxygen atmosphere for 30 minutes, 3 times. The Sm composition was varied from 0 (SBT) to 0.27. The P-V characteristics, drain current-gate voltage (I_D-V_G) characteristics, and XRD (X-ray diffraction) pattern of the samples were measured by RT66A (by Radiant Technologies Inc.), HP4156A (by Hewlett Packard Inc.), and MRD (by Phillips Inc.), respectively.

Table I. The fabrication procedure of SBT/SSBT capacitors.

Substrates:	
Pt(175nm) / Ti(20nm) / SiO_2 (100nm) / Si Supplied by Fujitsu	
Sol-gel solution:	
$Sr_{0.8}Bi_{2.2}Ta_2$ (SBT)	in 1-methoxy-2-buthanol
$Sr_{0.4}Sm_{0.27}Bi_{2.2}Ta_2$ (SSBT)	in 1-methoxy-2-buthanol
Other ratios mixing 2 solutions: Sr/Sm=0.7/0.07, 0.6/0.14, 0.5/0.21	
Supplied by Toshima Manufacturing Co., Ltd.	
Procedure:	
1. Spin-coat S(S)BT sol-gel solution	500rpm 5sec, then 2500rpm30sec
2. Drying	240°C, 10min, in air
3. Crystallization	750°C, 30min, in O_2
4. Repeat 1-3	3 times, 120nm
5. Deposit Pt top electrode	200μmφ, 60nm, e-beam deposition
6. Annealing	750°C, 10min, in O_2

Table II. The fabrication procedure of MFIS-FET.

Substrates:	
p-Si (100)	
Sol-gel solution:	
Same as those of Table I	
Procedure:	
1. Field oxidation	400nm, thermal oxidation
2. Transistor area formation	HF wet etching
3. S/D ion implantation	W/L=50/5μm, PH_3, 5x10¹⁶cm⁻², 20kV, annealed at 1000°C, 5min, in N_2
4. Insulator HfO_2 deposition	15nm, MOCVD (CET=10nm, increased by following several annealings)
5. SSBT formation	Sr/Sm/Bi/Ta=0.7/0.07/2.2/2, 170nm, sol-gel technique (same as Procedure 1-4 of Table I)
6. Pt gate electrode deposition	60nm, e-beam deposition
7. Contact hole formation	HF/HCl wet etching + Ar dry etching
8. Annealing	750°C, 10min, in O_2
9. Al S/D electrode deposition	130nm, resistance-heating deposition
10. Ag back electrode deposition	Resistance-heating deposition

4. RESULTS AND DISCUSSION

4.1 Ferroelectric capacitors

Figure 3 shows the P-E (polarization-electric field) hysteresis loops and x-ray diffraction patterns of SSBT films whose Sr/Sm ratio is 0.8/0, 0.7/0.07, 0.6/0.14, 0.5/0.21, and 0.4/0.27, respectively. As shown in Fig. 3, it is found that when the Sm composition increases, diffraction peaks from *c*-axis oriented crystallites such as (006), (008), (0010), and (0012) appear, and remanent polarization decreases. It is known that the SBT-based materials have small remanent polarization along the *c*-axis. We also observed the drastic change of the shape of the P-E hysteresis loops when the Sm composition is increased from 0.07 to 0.21. Although small remanent polarization was obtained for the SSBT films with Sm composition of 0.21 and 0.27, unfortunately, the saturation characteristics of the P-E hysteresis loops were degraded. From these results, we used the SSBT film with a Sr/Sm ratio of 0.7/0.07 for the MFIS-FET fabrication because it has well-saturated P-E loops and a smaller remanent polarization than SBT (Sr/Sm=0.8/0).

4.2 MFIS transistors

Figure 4 shows the I_D-V_G characteristics of the MFIS transistor with a fixed drain voltage of V_D=0.1V. V_G was swept from -6V to +6V and then from +6V to -6V. Here, we indicate this as $|V_{Gmax}|$=6V. The curves of $|V_{Gmax}|$=5V, 4V, and 3V are also shown. Throughout this paper, V_D is fixed to 0.1V for the I_D-V_G measurements. It was found that the memory window increases with the gate voltage. The memory windows are 0.71V, 0.54V, 0.31V, and 0.16V for $|V_{Gmax}|$=6V, 5V, 4V, and 3V,

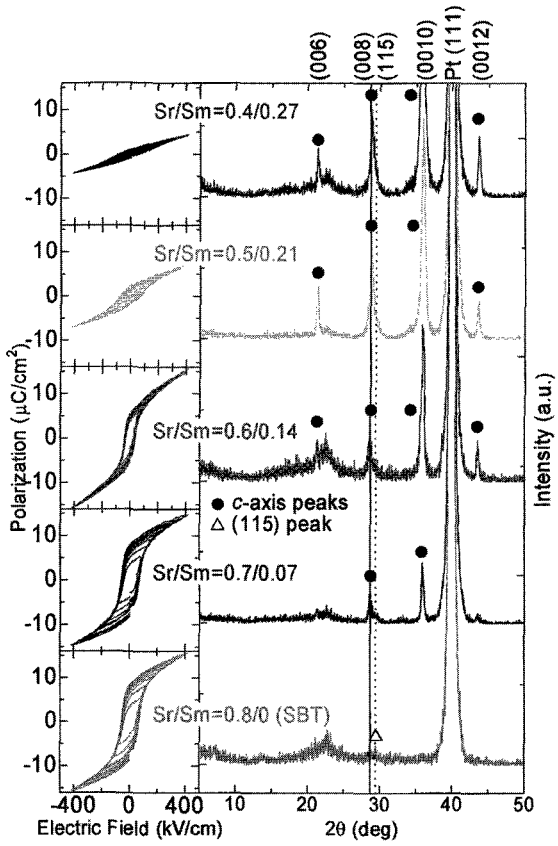

Fig. 3 P-E characteristics and XRD patterns of Pt/S(S)BT/Pt capacitors.

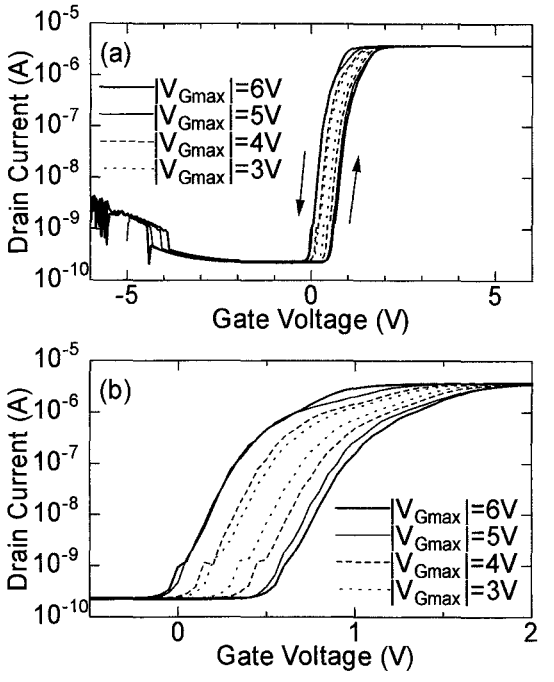

Fig. 4 The I_D-V_G characteristics of MFIS-FET. (b) is the enlarged figure of (a).

respectively. The appropriate read-out voltage V_{Gread} is 0.4V for $|V_{Gmax}|$=6V and 5V, because large ON/OFF ratio can be obtained at this read-out voltage.

Figures 5(a)-(c) show I_D-V_G curves, which simulate the read-out operations of the MFIS transistor. The dotted lines are the same as a whole loop shown in Fig. 4. The solid lines represent the measurement of I_D with sweeping V_G as (a) -5V(pulse) → 0V → +5V → 0V, (b) +5V → 0V → +5V, and (c) +5V(pulse) → (20 s pause) → 0V → +5V → 0V. The region from V_G=0V to V_G=V_{Gread}=0.4V of each figure corresponds to the read-out operation. The I_D-V_G curve shown in Fig. 5(a) is the same as the I_D-V_G curve originally measured, as shown in Fig. 4. This means that the read-out current

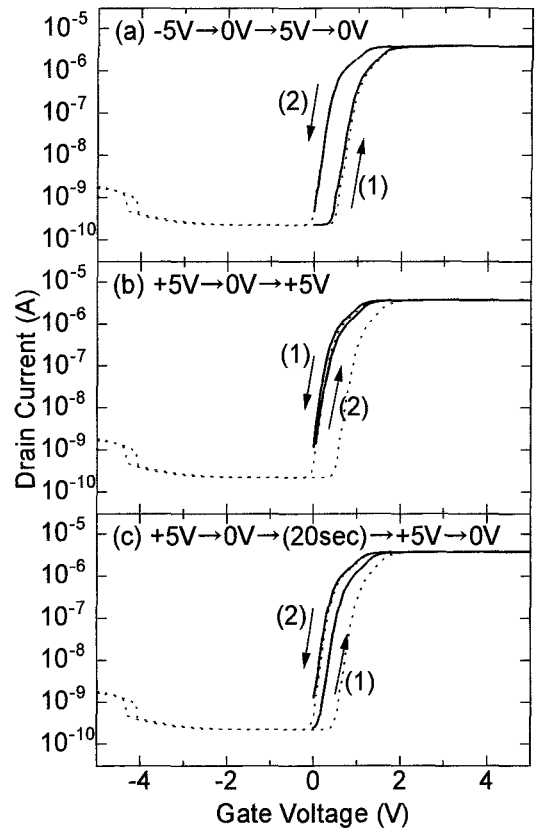

Fig. 5 The reading operation of the MFIS transistor:
(a) read-out in the OFF state,
(b) read-out in the ON state immediately after writing,
(c) read-out in the ON state after a 20 s pause.

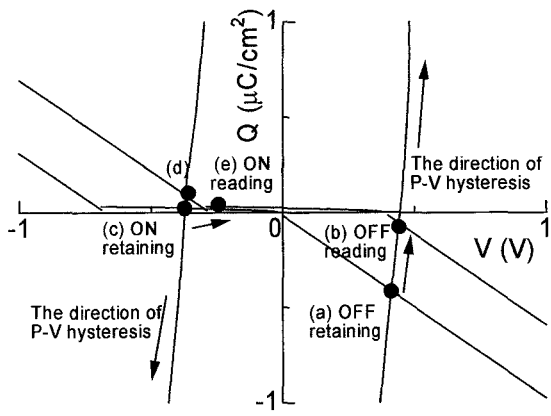

Fig. 6 The operation point analysis of MFIS-FET.

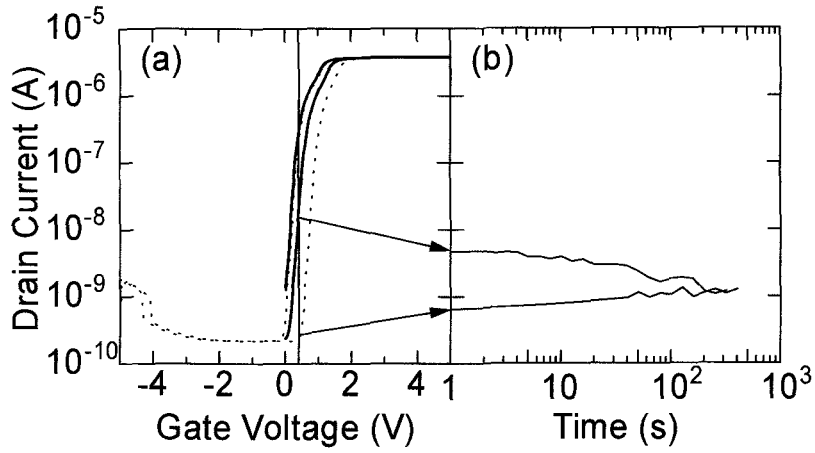

Fig.7 The retention property of the MFIS transistor:
(a) the ON reading curve (same as Fig. 5(c)) and (b)the reading curve

is not degraded when we read-out the OFF state. On the other hand, we can see from Figs. 5(b) and 5(c) that the drain current for the read-out operation is smaller than that of the whole curve shown in Fig. 4 and the degradation of the read-out current is more pronounced if the device is retained at V_G=0V for 20 s.

This degradation can be explained by Fig. 6. When the OFF state is retained, the operation point exists at (a) point in the fourth quadrant. When the OFF state is read out, the operation point moves along the hysteresis loop and reaches point (b). The movement is along the hysteresis loop; therefore, there is no difference in I_D-V_G curve. On the contrary, when the ON state is retained, the operation point exists at point (c) in the second quadrant. When the ON state is read out, if the operation point moves back on the hysteresis loop and reaches point (d), there is no degradation in drain current. However, the operation point actually moves to point (e), because the movement direction is opposite the P-V hysteresis loop. Therefore, the drain current to read out the ON state is smaller than that of the whole loop originally measured as shown in Fig. 4. To avoid the degradation of the read-out current, the split-gate structure is effective as we previously reported[13].

Figure 7 shows the retention property of the fabricated MFIS transistor. We measured the time dependencies of drain currents under the condition of V_G=0.4V and V_D=0.1V after applying V_G=5V or V_G=-5V. The drain current when we read out the ON state decreases with time. In addition, even when the OFF state is read out, the drain current slightly increased with time. Consequently, the ON/OFF current ratio becomes 1 after 200 s in this sample. The reason for the short retention time is not fully understood, but presumably one of the reasons is the use of a small minor loop, as well as the leakage current of the ferroelectric film.

5. CONCLUSION

Ferroelectric $Sr_{0.7}Sm_{0.07}Bi_{2.2}Ta_2O_9$ thin films were fabricated for low voltage operation of ferroelectric-gate transistors. It was found that the remanent polarization decreases with increasing Sm composition. However, the saturation of P-V hysteresis loops was also degraded. We then fabricated MFIS-FETs using a SSBT film with a Sm composition of 0.07 and low voltage operation was examined. It was found that the read-out drain current was degraded when we read out the ON state, whereas no degradation was observed to read out the OFF state.

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