Transactions of the Materials Research Society of Japan 32[1] 23-26 (2007)

Effect of TiO_2 Anatase Layer for $Bi_4Ti_3O_{12}$ Thin Film Prepared on $La_{0.05}Sr_{0.95}TiO_3$ Substrate

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$Bi_4Ti_3O_{12}$ (BIT) thin films with TiO_2 anatase layer were prepared on $La_{0.05}Sr_{0.95}TiO_3$ (LSTO) substrates by metalorganic vapor deposition using $Bi(CH_3)_3$ and $Ti(i\text{-}OC_3H_7)_4$ sources. When the substrate temperature was fixed at 500°C, the BIT thin films exhibited highly *c*-axis orientation. The *c*-axis orientation does not depend on layer created on LSTO substrate. The grain size of BIT thin film with TiO_2 anatase layer is smaller than that with of BIT thin film with no-layer. The grain size of the BIT thin film accords with that of TiO_2 anatase layer. This indicates that the TiO_2 anatase layer acts not as barrier layer but as an initial nucleation layer of the BIT thin film. The postannealed BIT thin film with TiO_2 anatase layer exhibited random orientation and *P-E* hysteresis loop.

Key words: $Bi_4Ti_3O_{12}$(BIT), thin film, TiO_2 layer, $La_{0.05}Sr_{0.95}TiO_3$ (LSTO) Substrate, MOCVD

1. INTRODUCTION

Bismuth layer-structured ferroelectrics $Bi_4Ti_3O_{12}$ (BIT) thin film is expected for application to nonvolatile ferroelectric memory (NV-FeRAM) devices with nondestructive readout operation due to its excellent fatigue endurance when in the deposition of this film with Pt electrode. The BIT has a spontaneous polarization in the *a-c* plane at an angle of about 4.5 ° to the *a*-axis, and exhibits two independently reversible components along the *c*- and a-axis [1-4]. It shows coercive fields (E_c) of 3.5 kV/cm and 50 kV/cm, remanent polarization (P_r) values of 4.0 μC/cm^2 and 50 μC/cm^2 along the *c*- and *a*-axes, respectively. The large P_r of *a*-axis takes advantage of reducing the memory cell area of a NV-FeRAM. The formation process at low temperature below 500 °C is desirable for the realization of poly-Si plug stacked capacitor memory cells [5-12]. This is because inter diffusion occurs between the electrode and poly-Si plug during ferroelectric film formation at high temperature.

In recent years, Nakamura *et al.* and co-workers have prepared the BIT thin films with a TiO_2 anatase layer on the Pt/Ti/SiO_2/Si substrates by metalorganic chemical vapor deposition (MOCVD) [13-16]. The BIT thin film with the TiO_2 anatase layer exhibited highly *a*- and *b*-axes-oriented BIT single phases, although the BIT thin film with no-layer exhibited a *c*-axis orientation. The interface between the BIT thin film and the substrate was very smooth. The BIT thin film consisted of small grains. The structural and ferroelectric properties of the BIT thin film with the TiO_2 anatase layer strongly depends on the thickness ratio of the BIT thin film to the TiO_2 anatase layer. Although the BIT thin film with TiO_2 anatase layer exhibited a good *P-E* hysteresis loop with large remanent polarization, the leakage current and surface morphology were not improved by inserting TiO_2 anatase layer.

In this study, we have prepared the BIT thin films with TiO_2 anatase layer by MOCVD. The (100)-oriented $La_{0.05}Sr_{0.95}TiO_3$ (LSTO) single crystals were used as the substrates of the thin films. It is known that the conductivity of $SrTiO_3$ can control by substituting La ions into Sr site. The LSTO used in this study is semiconductor. Therefore, LSTO is better substrate than Pt/Ti/SiO_2/Si substrate in order to prevent the interdifussion. In this paper, we present the structural and ferroelectric properties of the BIT thin films with a TiO_2 layer and discuss about the effect of TiO_2 layer.

2. EXPERIMENTAL

The TiO_2 anatase layers were prepared on (100) LSTO substrates by MOCVD. Tetra-isoproxy titanium [$Ti(i\text{-}OCH_3H_7)_4$], which was supplied by TRI Chemical Laboratory Inc, was used as the Ti source of MOCVD. The pressure in reaction chamber was fixed at approximately 5 Torr. The $Ti(i\text{-}OCH_3H_7)_4$ vaporized in a separate stainless-steel bubbler was maintained at 40°C. The substrate temperature (Ts) was approximately 350°C.

BIT thin films were deposited on the TiO_2 Anatase layer prepared on LSTO substrates by MOCVD using an apparatus having a vertical cold-wall-type reaction chamber. Trimethyl bismuth [$Bi(CH_3)_3$] and $Ti(i\text{-}OCH_3H_7)_4$ were used as Bi and Ti sources of MOCVD. The $Bi(CH_3)_3$ and $Ti(i\text{-}OCH_3H_7)_4$ vaporized in separate stainless-steel bubblers were maintained at 0°C and 40°C, respectively.

The Ar and O_2 gases were used as the carrier gas and oxidizing gas, respectively. The pressure in the reaction chamber was fixed at approximately 5 Torr. The Ts was fabricated at 500°C in all BIT thin films. The thickness of the BIT thin films was fixed at 300 nm. Finally, the top Pt electrodes with a diameter 0.2 mm were deposited on the film surface through a metal shadow mask by rf-magnetorn sputtering in order to measure electrical properties.

The structural properties of the BIT thin films were characterized by X-ray diffraction (XRD) using CuKα. The surface morphology was observed by atomic force microscopy (AFM). The polarization-electric field (*P-E*) hysteresis loops were measured using one-shot triangular waveforms with a period of 50 ms.

3. RESULTS AND DISCUSSION

Figure 1 (a) shows the XRD pattern of the as-deposited TiO_2 Anatase thin film prepared at Ts =350 °C. The film thickness of the TiO_2 layer was approximately 50nm. A peak at 2θ~46.5° is LSTO (200) peak. A sharp peak at 2θ~41.8° is Kβ line of X-ray. A weak peak at 2θ=38.5 ° is TiO_2 Anatase (004) peak. In recent years, TiO_2 anatase thin film has been prepared on $SrTiO_3$ substrates by magnetron sputtering [17]. The TiO_2 anatase shows highly *c*-axis orientation on (100)-oriented $SrTiO_3$ substrate. The lattice constants of $SrTiO_3$ and LSTO were about the same. Therefore, the *c*-axis orientation of TiO_2 thin film on LSTO accords with that of TiO_2 thin film on $SrTiO_3$.

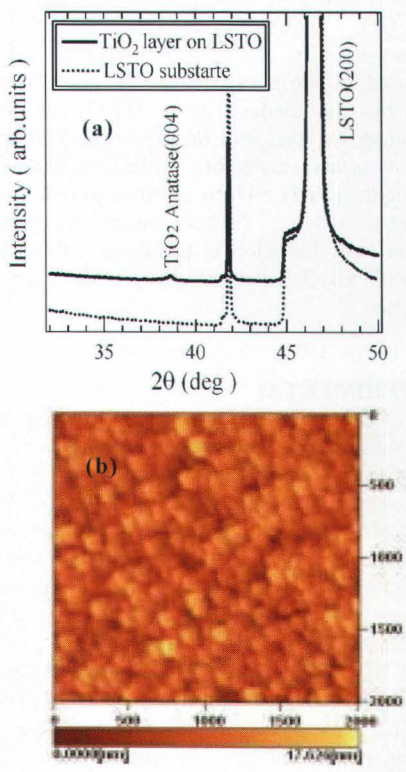

Fig. 1: (a) XRD pattern of TiO_2 anatase thin film (solid line) prepared on LSTO substrate. As reference, the XRD pattern of LSTO substrate is also shown as dashed line. (b) AFM image of TiO_2 anatase thin film prepared on LSTO substrate.

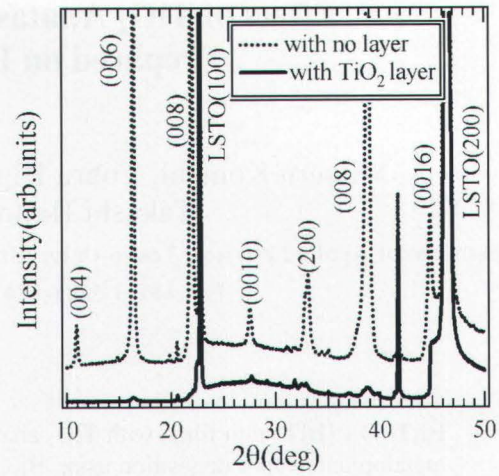

Fig. 2: XRD patterns of as-deposited BIT thin films with TiO_2 anatase layer and no-layer.

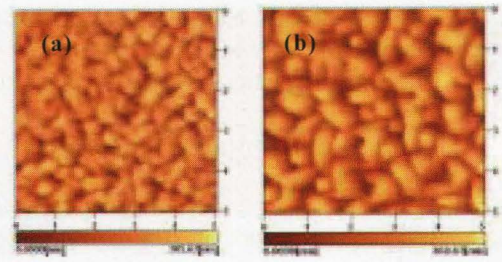

Fig. 3: AFM images of as-deposited BIT thin films with (a) TiO_2 anatase layer and (b) no-layer.

Figure 2 shows the XRD patterns of the as-deposited BIT films with the anatase layer and with no layer. The Ts and deposition pressure of these films were fixed at 500°C and 5 Torr, respectively. These total film thicknesses were approximately 300 nm. Both films exhibit highly *c*-axis orientation, although the (200) peak is also observed. The existence of other phase is not observed. Comparing each XRD pattern, the peak intensities are smaller in BIT thin film with TiO_2 anatase layer. This might be originated the difference of thickness of BIT thin film. On the other hand, it has been reported that the BIT thin film with TiO_2 layer on $Pt/Ti/SiO_2/Si$ substrate exhibits *a*- and *b*-axes oriented BIT single phase. The lattice parameters of TiO_2 anatase are a=0.378 nm and c=0.949 nm. The interval of oxygen ion distribution along (101) of TiO_2 anatase is close to the *a*- and *b*-axes lattice parameters than to the *c*-axis parameter of BIT. This difference originates to orientation of TiO_2 anatase thin film. The BIT thin film prepared in this study exhibits *c*-axis orientation on the (004)-oriented TiO_2 anatase layer from the concept of lattice matching.

Figure 3 shows the AFM images of BIT thin films with TiO_2 anatase layer and no-layer. The BIT thin fillm with TiO_2 anatase layer is higher density than BIT thin film with no layer. Furthermore, the grain size is smaller in BIT thin film with TiO_2 anatase layer. The grain size of the BIT thin film accords with that of TiO_2 layer, as shown in Fig. 1(b). This fact indicates that the

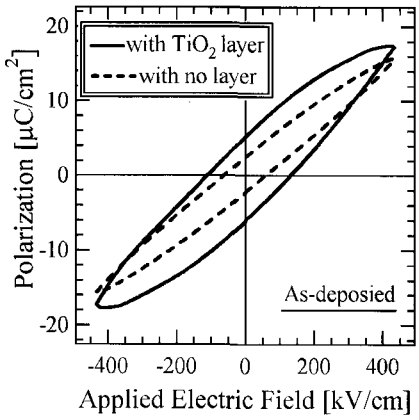

Fig. 4: *P-E* hysteresis loops of as-deposited BIT thin films with TiO_2 anatase layer (solid line) and no-layer (dashed line).

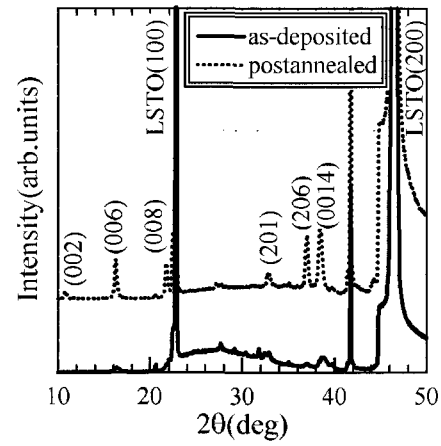

Fig.5: XRD patterns of as-deposited (solid line) and postannealed (dashed line) BIT thin films with TiO_2 anatase layer.

TiO_2 anatase layer acts not as barrier layer but as an initial nucleation layer of the BIT thin film.

Figure 4 shows *P-E* hysteresis loops of as-deposited BIT thin films with TiO_2 layer and no layer. These hysteresis loops were not saturated. This reason is due to the large leakage current of BIT thin film. Then, the leakage currents of BIT thin films with TiO_2 anatase layer and no-layer were 2×10^{-6} A/cm^2 and 3×10^{-5} A/cm^2, respectively. The large leakage currents of these BIT thin films originate to poor crystallization or oxygen vacancies.

Figure 5 shows XRD patterns of as-deposited and postannelaed BIT thin films with TiO_2 layers. The BIT thin film with TiO_2 anatase layer was annealed at 800°C for 1 h in order to compensate oxygen vacancies (postannelaed). The postannealed BIT thin film with TiO_2 anatase layer exhibits random orientation. The crystallization is higher in postannelaed BIT thin film with TiO_2 anatase layer.

Figure 6 shows the *P-E* hysterisis loop of as-deposited and postannelaed BIT thin films with TiO_2 layers. The shape of *P-E* hysteresis loop of BIT thin film with TiO_2 anatase layer was improved by postannealing. Furthermore, the remanent polarization (P_r) was also improved. The, the P_r and coercive field (E_c) were $2P_r$=26.6 μC/cm^2 and $2E_c$=340 kV/cm, respectively. The large E_c and poor saturation contribute to the remaining TiO_2 anatase layer, which acts as a low dielectric layer. Similar result has been reported in BIT thin film with TiO_2 anatase layer on Pt/Ti/SiO_2/Si substrate [16].

The above results are not enough for application of ferroelectric nonvolatile memories, which have stacked capacitor cell structures. However, the surface state and interdiffusion are controlled in BIT thin film with TiO_2 anatase layer on LSTO substrate. To further investigate the electrical properties of the BIT thin films on LSTO substrate, it is necessary to perform a more systematic optimizations of the film thickness of TiO_2 anatase layer and T_s.

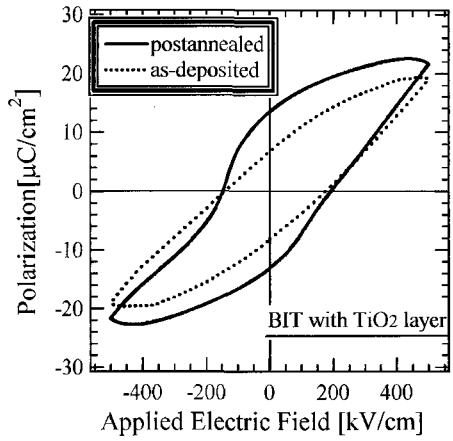

Fig.6: *P-E* hysteresis loops of as-deposited (dashed line) and postannealed (solid line) BIT thin films with TiO_2 anatase layer.

4. CONCLUSION

We have prepared the BIT thin films with TiO_2 anatase layer on LSTO substrates by MOCVD. When the substrate temperature was fixed at 500°C, the BIT thin films exhibited highly *c*-axis orientation, although the *c*-axis orientation does not depend on layer on LSTO substrate. The grain size of BIT thin film with TiO_2 anatase layer is smaller than that with of BIT thin film with no-layer. The grain size of the BIT thin film accords with that of TiO_2 anatase layer. This indicates that the TiO_2 anatase layer acts not as barrier layer but as an initial nucleation layer of the BIT thin film. The postannealed BIT thin film with TiO_2 anatase layer exhibited random orientation and good *P-E* hysteresis loop.

ACKNOWLEDGEMENTS

We would like to thank Mr. M. Saitoh and Mr. H. Shibata of Tokyo University of Science for their technical supports.

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(Received December 19, 2006;Accepted December 28, 2006)