Fabrication of Ferroelectric Gate Transistors with Sr(Ti,Ru)O₃ as a Channel

H. Fujisawa, S. Yoshida and M. Shimizu

Department of Electrical Engineering and Computer Sciences, Graduate School of Engineering, University of Hyogo 2167 Shosha, Himeji, Hyogo 671-2201, JAPAN

Fax: 81-79-267-4855, e-mail: fujisawa@eng.u-hyogo.ac.jp

We report electronic conduction of polycrystalline and epitaxial $Sr(Ti,Ru)O_3$ (STRO) thin films and fabrication of ferroelectric gate transistors using STRO as a channel and Pb(Zr,Ti)O₃ (PZT) as a ferroelectric gate insulator. Polycrystalline and epitaxial STRO films were prepared on SiO₂/Si and SrTiO₃(100) by sputtering using an STRO ceramic target (Ti/Ru=40/60). Hall effect measurements revealed that polycrystalline STRO films prepared at 560°C in a pure argon atmosphere had carrier densities of 10^{21} - 10^{22} cm⁻³ and mobilities of 0.1-0.3cm²V⁻¹s⁻¹, respectively. When STRO films were sputtered in a mixture of argon and oxygen gases, the carrier density decreased to an order of 10^{20} cm⁻³ due to an increase of Ti/Ru ratio. The mobility barely changed with an addition of oxygen. Epitaxial STRO films. Hall effect measurements also indicated that polycrystalline and epitaxial STRO films had *n*-type conduction. Ferroelectric gate transistors with a 6nm-thick-STRO layer as a channel showed a non-volatile field effect by two opposite polarization states of PZT. The change of channel conductance was approximately 40%.

Key words: Sr(Ti,Ru)O₃, Pb(Zr,Ti)O₃, ferroelectric gate transistors

1. INTRODUCTION

A field-effect-transistor (FET) with a ferroelectric gate oxide, such as metal/ferroelectric/semiconductor (MFS)-FET and metal/ferroelectric/insulator/ semiconductor (MFIS)-FET, has attracted much attention as a non-volatile memory device with a nondestructive read-out operation. [1] However, in MFS-FETs using silicon as a semiconductor, it is difficult to obtain an F/S interface with a low interface trap density because an interdiffusion or chemical reaction between ferroelectrics and semiconductors occurred during deposition of ferroelectrics at high temperature. In the MFIS-FETs, while a trap density of I/S interfaces can be reduced as compared with that of F/S interfaces, an insertion of insulators causes some other difficulties, such as a short retention time due to a depolarization field and high operation voltage. Therefore, very thin insulators with a low leakage current are required to obtain a long retention time and low voltage operation. [2]

On the other hand, thin-film-transistors (TFTs) with ferroelectrics as a gate insulator have also been studied. In TFTs, MFS-typed structure can be realized because difficulties caused by the incompatibility of ferroelectric with silicon in Si-based MF(I)S-FETs can be solved by using various conductors other than Si as a channel. In particular, MFS-typed TFTs are advantageous over Sibased MFIS-FETs in that depolarization fields are reduced by screening by carriers in the channel. When ferroelectric oxides are used as a gate insulator of MFStyped TFTs, conductive oxides, such as (In,Sn)O_x (ITO), ZnO, (La,Ca)MnO₃, SrRuO₃ (SRO), Sr(Ti,Ru)O₃ (STRO), are suitable for channel materials. [3-7] Among these conductive oxides, STRO, which is a solid solution of insulative SrTiO₃ (STO) and conductive SRO, is one of promising materials for a channel in a ferroelectric gate FETs because STRO has a perovskite structure with lattice parameters close to perovskite-typed ferroelectrics and conductivity can be controlled by changing Ti/Ru ratio. [6-9] For example, Kuffer et al. and Schrott et al. reported resistivity modulations of 75% and 36% in TFTs with STRO channel and Pb(Zr,Ti)O₃ (PZT) gate insulator, respectively. [4,6] However, there have been a few reports on details of conduction of STRO films including the carrier type, carrier density and mobility. [7-9] In particular, both nand p- type conductions were reported for not only STRO but also SRO films. [3,4,6,10]

In this study, we prepared polycrystalline and epitaxial STRO films on SiO_2/Si and STO(100) by sputtering and investigated electrical conduction by Hall effect measurements. Fabrication and characterization of epitaxial ferroelectric gate transistors using PZT as a gate insulator and STRO as a channel are also reported.

2. Experimental procedure

Epitaxial and polycrystalline STRO films were deposited on STO(100) and SiO₂/Si(100) by rfsputtering using an STRO ceramic target with Ti/Ru ratio of 40/60. The deposition temperature was changed from room temperature (RT) to 560°C. The sputtering power density and total pressure were fixed at 1.38W/cm² and 10mTorr with a mixture of argon and oxygen gases. The O₂ concentration was changed from 0 to 40% to control the conductivity of STRO films. Crystalline properties and chemical composition were examined by x-ray diffraction (XRD) and x-ray fluorescence (XRF) analyses, respectively. Carrier density and mobility of epitaxial and polycrystalline STRO films were measured by Hall effect



Fig.1 An epitaxial ferroelectric transistor with STRO, PZT and SRO as a channel, gate insulator, and bottom gate electrode, respectively.

measurements.

Ferroelectric gate transistors with a bottom gate structure were fabricated on STO(100) substrate, as shown in Fig.1. 60nm-thick epitaxial SRO films were prepared on STO(100) as a bottom gate electrode at 560°C by rf-sputtering using a stoichiometric SRO target. Sputtering pressure and O₂ concentration were 10mTorr and 5%, respectively. 200-300nm-thick epitaxial PZT thin films were prepared as a gate insulator at 560°C by metalorganic chemical vapor deposition (MOCVD) using (C₂H₃)₃PbOCH₂C(CH₃)₃, Zr(O-t-C₄H₉)₄, Ti(O-i-C₃H₇)₄ as precursors and O₂ as an oxidizer. 6nm-thick STRO channels were prepared at 560°C by rf-sputtering and patterned by lift-off method. Finally, Pt films was sputtered and patterned as source and drain electrodes. The channel length and width were 5-10 and 50-400µm, respectively.

3. RESULTS AND DISCUSSION

3.1 Preparation and characterization of STRO films

At the first stage, we sputtered 80-95nm-thick polycrystalline STRO films on SiO2/Si in a pure argon gas and investigated influences of deposition temperature on the crystallinity and conductivity. When STRO films were sputtered without substrate heating, STRO films showed no conductivity because of poor crystallinity. At deposition temperatures higher than 390°C, well-crystallized STRO films with random orientation were obtained. The resistivity of STRO films prepared at 390-560°C ranged from 7 to 13mΩ·cm. Hall effect measurements revealed that these STRO films were *n*-type conductors with a carrier density of 10^{22} cm⁻³ and Hall mobility of 0.1cm²V⁻¹s⁻¹. XRF analysis revealed that these STRO films had Ti/Ru ratio of 0.40, which agreed well with that of the sputtering target. Therefore, it was found that STRO films with a stoichiometric composition and high carrier density were obtained when STRO was sputtered above 390°C in the pure argon gas.

Thickness dependence of carrier density and mobility of STRO films prepared at 560°C in the pure argon gas was also evaluated. The carrier density and mobility of STRO films with thicknesses larger than 40nm were almost constant at 10^{22} cm⁻³ and 0.1cm²V⁻¹s⁻¹, respectively. The carrier density decreased to $\sim 10^{21}$ cm⁻³ and mobility slightly increased to 0.3cm²V⁻¹s⁻¹ with decreasing the thickness to 16nm.

From these experimental results, it was found that the carrier density of STRO films prepared in the pure argon



Fig.2 Dependence of carrier density and mobility on O_2 concentration of sputtering atmosphere.



Fig.3 A relationship between film compositions and O_2 concentration of sputtering atmosphere.

gas was too high to control the conductance of STRO films by ferroelectric polarizations of PZT thin films.

In the next stage, in order to increase Ti/Ru ratio and subsequently reduce the carrier density, oxygen gas was added to the sputtering gas. Figure 2 shows dependence of carrier density and mobility of polycrystalline STRO films prepared at 560°C on O2 concentration of the sputtering atmosphere. The thicknesses of STRO films were 12-14nm. The carrier density fell from 2×10^{21} to 3×10^{20} cm⁻³ as O₂ concentration increased from 0 to 10%. In the range of O_2 concentration from 10 to 40%, the carrier density slightly increased with O₂ concentration. On the other hand, the mobility barely varied with O_2 concentration. Figure 3 shows a relationship between film composition of STRO films and O2 concentration of sputtering gas examined by XRF analysis. When STRO films were sputtered in the mixture of argon and oxygen, Ti/Ru and Sr/(Ru+Ti) ratios were almost constant at 0.58 and 1.22, respectively, which was larger than those of films prepared in the pure argon atmosphere. These XRF results indicate that Ru was deficient in STRO films sputtered in the mixture of argon and oxygen gases because of high volatility of RuOx. [12] From these results, it was found that the change of the carrier



Fig.4 (a) P-V and (b) I-V curves measured between gate and source electrodes.

density by mixing oxygen gas to the sputtering gas was caused by an increase of Ti/Ru ratio although Sr deficiency was induced. In addition, the dependence of the carrier density on Ti/Ru ratio was similar to those of the first-principle calculations and experimental studies. [8,9]

Based on these experimental results on polycrystalline STRO films, 15nm-thick epitaxial STRO films were also prepared at 560°C on STO(100) substrate and the carrier density and mobility were evaluated. The total pressure and O_2 concentration were 10mTorr and 10%, respectively. Hall effect measurement indicates that a carrier density and mobility of epitaxial STRO films were 10^{20} cm⁻³ and 0.2 cm²V⁻¹s⁻¹, respectively, which were comparable with those of polycrystalline films.

3.2 Fabrication of ferroelectric gate transistors with STRO channel and PZT gate insulator

Ferroelectric gate transistors with bottom gate electrode were fabricated on STO(100) substrate using epitaxial STRO films as a channel. In order to fully control carriers in STRO channel with a carrier density of 10^{20} cm⁻³ by ferroelectric polarization of PZT films, the thickness is required to be smaller than 10nm because a remanent polarization of our epitaxial PZT films is approximately 30μ C/cm². Therefore, 6nm-thick STRO film was used. The structure of bottom gate-typed



Fig.5 $I_{\rm D}$ - $V_{\rm D}$ characteristics as a function of $V_{\rm G}$. $V_{\rm G}$ was applied for 30sec and $I_{\rm D}$ was measured after removing $V_{\rm G}$.

epitaxial ferroelectric transistors is shown in Fig.1.

P-V hysteresis and I-V curves measured between gate and source electrodes of Pt/STRO/PZT/SRO transistors are shown in Fig.4. The channel length and width are 10 and 50µm, respectively. Saturated P-V hysteresis loops were obtained at applied voltages larger than $\pm 3V$ although voltage shifts were observed. A remanent polarization and coercive voltage were 20-30µC/cm² and 1-2V, respectively. A gate leak current was less than 10⁻⁷A when the gate voltage was swept from -3 to +3V. This value is higher than the expected drain current calculated using dimensions and conductivity of STRO channel. Therefore, the drain current (I_D) - drain voltage (V_D) characteristics mentioned below were measured after removing the gate voltage (V_G).

Figure 5 shows $I_{\rm D}$ - $V_{\rm D}$ characteristics as a function of $V_{\rm G}$. The gate voltages of ±5V were applied for 30sec to switch the polarization completely. Subsequently, the drain current was measured by sweeping the drain voltage from 0 to +3V. As shown in Fig.5, field effects caused by two opposite polarization states of PZT thin film were clearly observed. The drain current measured after applying $V_{\rm G}$ of +5V was 40% larger than that measured after applying $V_{\rm G}$ of -5V. This means that STRO film successfully acted as an n-channel which expected from the results of Hall effect was measurements. In addition, the field effects observed were non-volatile effects because $I_{\rm D}\text{-}V_{\rm D}$ characteristics were measured after removing $V_{\rm G}$. The modulation of channel conductance obtained from a slope of $I_{\rm D}$ - $V_{\rm D}$ curves was ~40%. This is comparable with those reported for ferroelectric gate transistors with STRO channels, 75% in Ref.[4] and 36% in Ref.[6]. However, electrons in STRO films were not fully controlled by ferroelectric polarizations because the change of channel conductance experimentally obtained in this study was much smaller than the expected value. Possible reasons for this are a larger carrier density than the expected value, screening of field effects by a large number of carriers and poor crystallinity of STRO layers due to the deficiency of Ru.

For the further improvement of change of channel

conductance, therefore, fabrication of STRO channel with smaller thickness and stoichiometric composition using a target with large Ti/Ru ratio will be required.

4. CONCLUSIONS

Electronic conduction, including carrier type, density and mobility, of polycrystalline and epitaxial STRO films prepared on SiO₂/Si and STO(100) by sputtering were investigated. Polycrystalline STRO films showed *n*-type conduction with carrier densities of 10^{20} - 10^{22} cm⁻³ and mobilities of 0.1-0.3cm²V⁻¹s⁻¹. Epitaxial STRO films also showed the conduction properties similar to those of polycrystalline films. Based on these experimental results on the conduction of STRO films, epitaxial TFTs with PZT as a gate insulator were fabricatted. The STRO channels acted as *n*-channel and exhibited a non-volatile change of the conductance by two opposite polarization states of PZT. The change of channel conductance was 40% for TFTs using a 6nm-thick STRO channel.

ACKNOWLEGEMENTS

This work was supported in part by a Grant-in-Aid for Young Scientists (B) (18760238) from the Ministry of Education, Culture, Sports, Science and Technology, a Grant-in-Aid from the Japan Society for the Promotion of Science (B) (16340093, 17360144), and a research grant from The Sumitomo Foundation.

5. REFERENCES

- J. L. Moll and T. Tarui, *IEEE Trans. Electron.* Devices, 10, 338 (1963).
- [2] S. Sakai and R. Ilangovan, *IEEE Electron Device Lett.*, 25, 369 (2004).
- [3] C. H. Ahn, R. H. Hammond, T. H. Geballe, M. R. Beasley J.-M. Triscone, M. Decroux, O In . Fischer, L. Antognazza and K. Char, *Appl. Phys. Lett.*, 70, 206 (1997).
- [4] A. G. Schrott, J. A. Misewich, V. Nagarajan and R. Ramesh, *Appl. Phys. Lett.*, 82, 4770 (2003).
- [5] T. Miyasako, M. Senoo and E. Tokumitsu, *Appl. Phys. Lett.*, 86, 162902 (2005).
- [6] O. Kuffer and O. Fischer, J. Appl. Phys., 97, 014103 (2005).
- [7] L. Mieville and T. H. Geballe, L. Antognazza and K. Char, *Appl. Phys. Lett.*, 70, 126 (1997).
- [8] T. Shimizu and T. Kawakubo, Jpn. J. Appl. Phys., 40, L117 (2001).
- [9] T. Ohara, T. Schimizu, K. Sano, M. Yoshiki and T. Kawakubo, *Jpn. J. Appl. Phys.*, 40, 1384 (2001).
- [10] M. Hiratani, C. Okazaki, K. Imagawa and K. Takagi, Jpn. J. Appl. Phys., 35, 6212 (2001).
- [11] H. Nonomura, H. Fujisawa, M. Shimizu and H. Niu, Jpn. J. Appl. Phys., 41, 6682 (2002).
- [12] S. Kolesnik, Y. Z. Yoo, O. Chmaissem, B. Dabrowski, T. Maxwell C. W. Kimball and A. P. Genis, *J. Appl. Phys.*, 99, 08F501 (2006).

(Received December 9, 2006; Accepted December 25, 2006)