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MD Simulation of Defect Generation during Annealing Process of Copper Wiring

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In the production of LSI, annealing process is necessary to coarsen the crystal grains in the wire. In this process, the wiring breakdown is frequently caused by the defect generation in the bottom of the buried wire. To overcome this difficulty, we investigated the conditions for the defect generation and the atomic behavior during the annealing process by the molecular dynamics simulation. Three rigid plates are placed as the two sidewalls and the bottom of the wire with a rectangular parallelepiped shape. A single crystalline copper is placed as the material of the wiring and the covered layer. After the relaxation at a low temperature for the structural stabilization, an annealing temperature is set for the sample. Calculation parameters are the annealing temperature, the thickness of the covered layer, the width, the height and the strain of the wire. It was shown that defect generations are suppressed when the annealing temperature is lower, the dimension of the wire is larger and the compressive strain is larger. These results coincide with the tendency of the real experiments.
Key words: simulation, MD, LSI, wire, defect

1. INTRODUCTION

Copper is generally adopted as the material of the wiring in LSI instead of aluminum to decrease the electrical resistance. Prominent production techniques is required for the copper interconnect on the patterned insulators layer because the copper film cannot be patterned as interconnect by the conventional etching process for the aluminum film [1,2]. The damascene process is commonly utilized to prepare the multi-layer structure composed of the copper interconnect and the insulator [3,4]. In this process, the covered layer on the wire is removed after the copper deposition on the patterned insulators layer [5,6].

After the deposition of the copper layer, the annealing process is necessary to coarsen the crystal grains in the wire. Coarse crystal grains induce the increase of the strength of electromigration and the decrease of the electrical resistance [7,8]. However, the wiring breakdown is frequently caused by the defect generation in the bottom of the buried wire in this process. To overcome this difficulty, we investigated the conditions for the defect generation and the atomic behavior during the annealing process by the molecular dynamics (MD) simulation.

2. METHODS OF CALCULATION

2.1 Model

In the present study, the specimen is composed of the substrate, the wire and the covered layer. As the substrate mimicking the patterned insulators layer, three rigid plates are placed as the two sidewalls and the bottom of the wire with a rectangular parallelepiped shape. Then, a single crystalline copper is placed as the material of the wiring and the covered layer. The vertical direction of the covered layer is set as the free boundary, and other directions are set as the periodic boundary.

After the relaxation at a low temperature for the structural stabilization, an annealing temperature is set for the sample. Temperature is controlled with the ad hoc velocity scaling. Relaxation time and annealing time are 30 ps and 70 ps, respectively. Calculation parameters are the annealing temperature, the thickness of the covered layer, the width, the height and the strain of the wire. The number of atoms is determined by the thickness of the covered layer, the width of the wire and the height of the wire, and the strain of the wire corrects the volume of the wire.

2.2 Sample

The number of fcc unit lattices at the parallel direction of the wire, the vertical direction of the wire and the vertical direction of the covered layer is 8, 12 and 13, respectively. Then, its structure is excised following the substrate shape determined by the calculation parameters. Sample size is 2.89 × 4.33 × 4.69 nm, and the number of atoms is about 1,800.

Time integral of the atomic motion is calculated by the velocity Verlet method in Eq. 1.

$$\mathbf{r}_i(t+\Delta t) = \mathbf{r}_i(t) + \Delta t \mathbf{v}_i(t) + \frac{(\Delta t)^2}{2m_i}\mathbf{F}_i(t),$$
$$\mathbf{v}_i(t+\Delta t) = \mathbf{v}_i(t) + \frac{\Delta t}{2m_i}[\mathbf{F}_i(t+\Delta t) + \mathbf{F}_i(t)], \quad (1)$$

$\mathbf{r}_i$, $\mathbf{v}_i$, $\mathbf{F}_i$, and m_i are the position, velocity, force and mass of atom i. Δt is the proceeding time during 1 step calculation, and is set to 1 fs.

2.3 Potential

The interaction between atoms is calculated by the extended Tersoff potential [9,10]. This potential is based on the Tersoff potential, and can reproduce the energy of the semiconductor, metal, oxide and other compounds [11,12]. Equations of the extended Tersoff potential are

shown in Eq. 2.

$$
\begin{aligned}
&U_T = \sum_{i<j} u_{ij} + \sum_i \phi_i, \\
&\phi_i = \left[(I_{Ei} + A_{Ei})/(2e)\right]q_i + \left[(I_{Ei} - A_{Ei})/(2e^2)\right]q_i^2, \\
&u_{ij} = u_{REPij} + u_{SHTij} + u_{IONij} + u_{VDWij}, \\
&u_{REPij} = f_{Sij} A_{ij} \exp(-\lambda_{ij} r_{ij}), \\
&u_{SHTij} = -f_{Sij} b_{ij} B_{ij} \exp(-\mu_{ij} r_{ij}), \\
&u_{IONij} = f_{Lij} \eta_i \eta_j q_i q_j / (4\pi\varepsilon_0 r_{ij}), \\
&u_{VDWij} = -f_{Lij} \sqrt{(C_{VDWi} C_{VDWj})} / r_{ij}^{\,6},
\end{aligned}
\tag{2}
$$

where

$$
\begin{aligned}
&b_{ij} = \left[1 + (\beta_i \sum_k \zeta_{ijk})^{n_i}\right]^{-1/(2n_i)}, \\
&\zeta_{ijk} = f_{Sik} \exp\left[\mu_{ij}^{\,m_i} (r_{ij} - r_{ik})^{m_i}\right] \\
&\qquad \times \left\{1 + c_i^2/d_i^2 - c_i^2/\left[d_i^2 + (h_i - \cos\theta_{ijk})^2\right]\right\}, \\
&f_{Sij} = f_c(r_{ij}, \sqrt{R_{Si} R_{Sj}}, \sqrt{S_{Si} S_{Sj}}), \\
&f_{Lij} = f_c(r_{ij}, \sqrt{R_{Li} R_{Lj}}, \sqrt{S_{Li} S_{Lj}}), \\
&f_c(r,R,S) = \begin{cases} 1, & (r \le R) \\ 1/2 + (1/2)\cos\left[\pi(r-R)/(S-R)\right], & (R < r < S) \\ 0, & (r \ge S) \end{cases} \\
&\lambda_{ij} = (\lambda_i + \lambda_j)/2, \\
&\mu_{ij} = (\mu_i + \mu_j)/2, \\
&A_{ij} = \sqrt{A_{Si} A_{Sj}}, \\
&B_{ij} = \sqrt{B_{Si} B_{Sj}}, \\
&A_{Si} = A_i \exp(\lambda_i D_i), \\
&B_{Si} = B_i \exp(\mu_i D_i)\left[a_{Bi} - | b_{Bi}(q_i - Q_{Oi}) |^{n_{Bi}}\right], \\
&D_i = D_{Ui} + | b_{Di}(Q_{Ui} - q_i) |^{n_{Di}}, \\
&b_{Di} = (D_{Li} - D_{Ui})^{1/n_{Di}} / (Q_{Ui} - Q_{Li}), \\
&n_{Di} = \ln[-D_{Ui}/(D_{Li} - D_{Ui})] / \ln[Q_{Ui}/(Q_{Ui} - Q_{Li})], \\
&b_{Bi} = | a_{Bi} |^{1/n_{Bi}} / \Delta Q_i, \\
&a_{Bi} = 1/(1 - | Q_{Oi}/\Delta Q_i |^{n_{Bi}}), \\
&Q_{Oi} = (Q_{Ui} + Q_{Li})/2, \\
&\Delta Q_i = (Q_{Ui} - Q_{Li})/2,
\end{aligned}
\tag{3}
$$

The potential energy of the system U_T is calculated as the summation of repulsive energy u_{REPij}, short-range energy u_{SHTij}, ionic bond energy u_{IONij}, van der Waals energy u_{WDWij} and the energy of atom i itself ϕ_i. q_i is the charge of atom i, and is optimized at every step to minimize U_T. In the present study, the charge optimization is omitted because the interaction by the charge does not exist in the single substance. Other parameters are set as Eq. 4.

$$
\begin{aligned}
&A\,(10^{-18}\text{J}) = 128.5, \quad B\,(10^{-18}\text{J}) = 6.92, \\
&\lambda\,(10^{10}\text{m}^{-1}) = 2.83, \quad \mu\,(10^{10}\text{m}^{-1}) = 1.412, \\
&\beta = 0, \quad n = 1, \quad m = 1, \\
&c = 0, \quad d = 1, \quad h = 0, \\
&R_S\,(10^{-10}\text{m}) = 2.82, \quad S_S\,(10^{-10}\text{m}) = 3.33, \\
&R_L\,(10^{-10}\text{m}) = 1.1, \quad S_L\,(10^{-10}\text{m}) = 5.0, \\
&I_E/e\,(\text{J/C}) = 7.72, \quad A_E/e\,(\text{J/C}) = 0.90, \\
&Q_L = -6, \quad Q_U = 2, \\
&D_L\,(10^{-10}\text{m}) = 1.49, \quad D_U\,(10^{-10}\text{m}) = -1.12, \\
&n_B = 10, \quad \eta = 1, \quad C_{VDW}\,(\text{Jm}^6) = 0,
\end{aligned}
\tag{4}
$$

The interaction between atoms and rigid plates is calculated by the Morse potential to save calculation time [13]. Equation of the Morse potential is shown in Eq. 5, and parameters are set as Eq. 6.

$$
\phi_{ij} = D\left\{\exp\left[-2\alpha(r_{ij} - r_0)\right] - 2\exp\left[-\alpha(r_{ij} - r_0)\right]\right\}, \tag{5}
$$

$$
\begin{aligned}
&D\,(10^{-18}\text{J}) = 0.0697, \quad \alpha\,(10^{10}\text{m}^{-1}) = 4.6487, \\
&r_0\,(10^{-10}\text{m}) = 1.9475,
\end{aligned}
\tag{6}
$$

3. RESULTS AND DISCUSSION

Simulating results are visualized to detect the defect generation. Fig. 1 represents the change of atomic arrangements with the 2% compressive strain. The void was absent in the bottom of the wire. The covered layer was attracted into the wire, and the wire was divided to several grain structures. It is considered that the defect was not generated because the local strain remained in the wire.

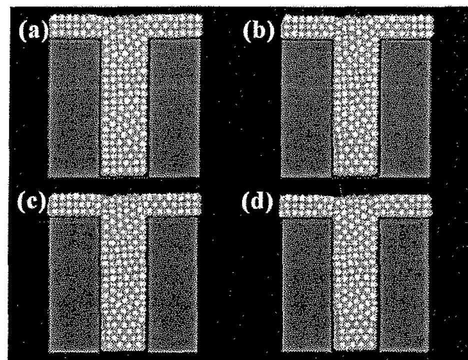

Fig. 1 Change of atomic arrangement with 2 % compressive strain. (a)-(d) are arrangements at 30 ps, 32 ps, 34 ps and 36 ps, respectively.

In contrast, Fig. 2 represents the change of atomic arrangements with the 1% tensile strain. The void existed in the bottom of the wire. The top of the covered layer became flat from concave, and the atomic arrangement in the wire became ordered more than the case of Fig. 1. It is considered that the local strain relaxed by the defect generation. In this manner,

simulating results were classified as defect suppression or defect generation.

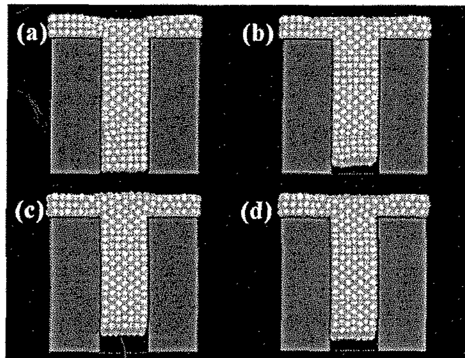

Fig. 2 Change of atomic arrangement with +1 % tensile strain. (a)-(d) are arrangements at 30 ps, 32 ps, 34 ps and 36 ps, respectively.

Fig. 3 represents the relationships between the strain and the annealing temperature. Open square and filled circle represent the defect suppression and the defect generation, respectively. The more defects were generated when the annealing temperature was higher and the tensile strain was larger. The influence of the strain to the defect generation was larger than of the annealing temperature. It is shown that the wire material should be packed densely to avoid defect generation.

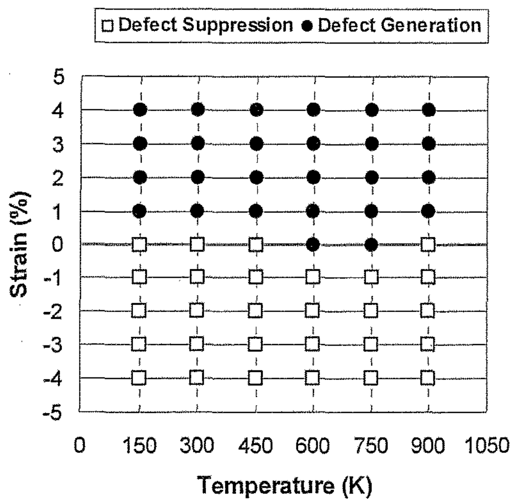

Fig. 3 Relationship between strain and annealing temperature. Open square and filled circle represent the defect suppression and the defect generation, respectively.

Fig. 4 represents the relationships between the height of the wire and the annealing temperature. The more defects were generated when the annealing temperature was higher and the height of the wire was smaller, defect suppressions alternately appeared to the height of the wire. It is considered that the appropriate height of the wire exists in atomic level because the adhesive strength differs in the atomic plane contacting the bottom of the wire.

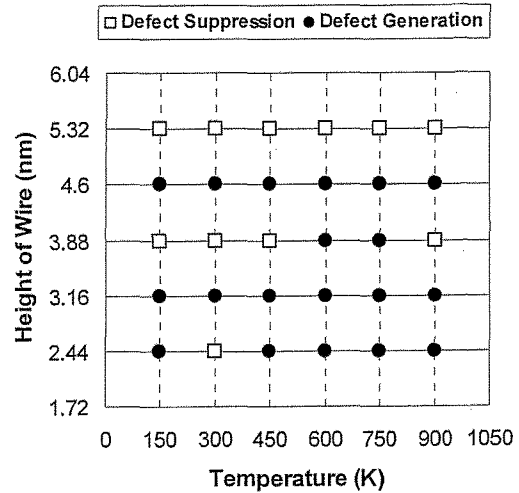

Fig. 4 Relationship between height of wire and annealing temperature. Open square and filled circle represent the defect suppression and the defect generation, respectively.

Fig. 5 represents the relationships between the width of the wire and the annealing temperature. The more defects were generated when the annealing temperature was higher and the width of the wire was smaller. It is considered that the defect generation is suppressed with the large dimension of the wire because the large wire can relax local strain.

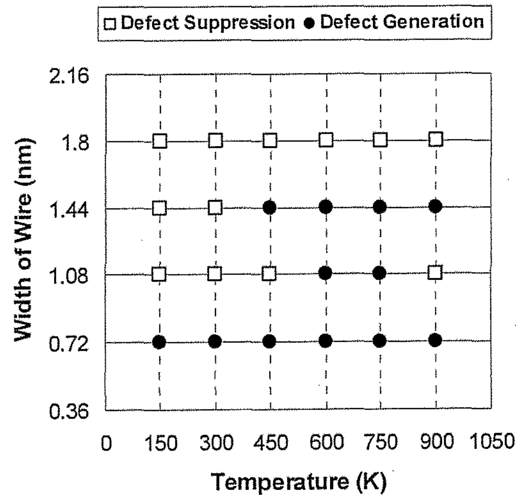

Fig. 5 Relationship between width of wire and annealing temperature. Open square and filled circle represent the defect suppression and the defect generation, respectively.

Fig. 6 represents the relationships between the thickness of the covered layer and the annealing temperature. The more defects were generated when the annealing

temperature was higher and the covered layer is thicker. Since the thin covered layer cannot distort, it is considered that the thin covered layer cannot act the net force the wire that creates large void.

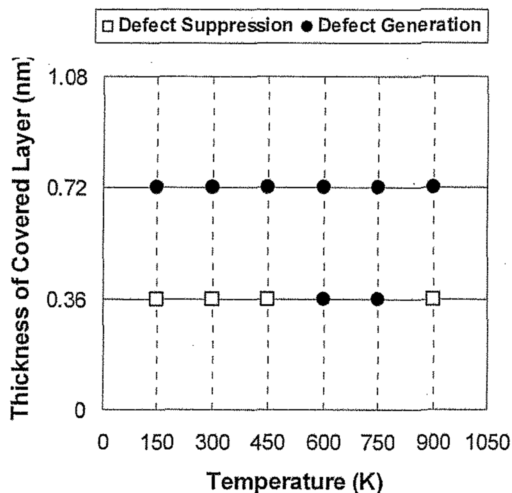

Fig. 6 Relationship between thickness of covered layer and annealing temperature. Open square and filled circle represent the defect suppression and the defect generation, respectively.

4. CONCLUSIONS

By using a molecular dynamics method, computer simulations of an annealing process on the copper wiring in LSI were performed. Calculation parameters are the annealing temperature, the thickness of the covered layer, the width, the height and the strain of the wire. Simulating results were classified as defect suppression or defect generation by visualized results, and were arranged as the relationships between each parameter and the annealing temperature. The results obtained are summarized as follows.

(1) Lower the annealing temperature, defect generation is suppressed. However, this effect is smaller than effects of other parameters.
(2) Larger the compressive strain, defect generation is suppressed. Therefore, the wire material should be packed densely to avoid defect generation.
(3) Larger the dimension of the wire, defect generation is suppressed. It is considered that the large wire can relax local strain.
(4) Thinner the covered layer, defect generation is suppressed. Since the thin covered layer cannot distort, it is considered that the thin covered layer cannot act the net force the wire that creates large void.

5. REFERENCES

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